DESIGN OF A HIGH PRECISION OPERATIONAL AMPLIFIER USING PING PONG AUTO ZERO ARCHITECTURE

A THESIS SUBMITTED IN PARTIAL FULFILLMENT

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By

Prasant Choudhury

Roll No: 210EC2308

Under the guidance of

Prof. K. K. Mahapatra

Department of Electronics & Communication Engineering

National Institute of Technology

Rourkela

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National Institute Of Technology

Rourkela

CERTIFICATE

This is to certify that the thesis entitled, "DESIGN OF A HIGH PRECISION OPERATRIONAL AMPLIFIER USING PINGPONG AUTOZERO ARCHITECTURE" submitted by Prasant Choudhury (210ec2308) in partial fulfilment of the requirements for the award of Master of Technology degree in Electronics and Communication Engineering with specialization in "VLSI design & Embedded systems" during session 2010-2012 at National Institute Of Technology, Rourkela (Deemed University) and is an authentic work by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any Degree or Diploma.

Prof K.K Mahapatra

Dept. of Electronics and Communication Engineering

National Institute of Technology Rourkela

Dedicated to my parents and well wishers

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PRASANT CHOUDHURY

210EC2308

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Abstract

A wide variety of electronic applications deal with small signal inputs. These systems need to have very low offset as well as very low offset drift over time and temperature. High precision is required in these fields. Such fields like instrumentation, automotive and industrial applications require precision amplifiers within reasonable cost and simplicity. The amplifiers by far having the lowest possible offset and offset drift is the auto zero amplifier.

In this thesis we describe a precision opamp using ping pong auto zero architecture , which is capable of very low offset and offset drift over temperature along with producing continuous output. The architecture has been designed to operate in extreme environments under a wide temperature. The simulated results show that the amplifier is fully functional and capable of less than 15uV of input referred offset voltage. The design has been carried out in cadence 0.18um technology. It consumes 4.2mW of power and has a offset drift over temperature 3.5uV/^{0}C.

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Abbreviations used

OPAMP	Operational Amplifier
CMRR	Common Mode Rejection Ratio
ICMR	Input Common Mode Range
PSRR	Power Supply Rejection Ratio
S&H	Sample and Hold
NMOS	N-type metal oxide semiconductor
PMOS	P-type metal oxide semiconductor
dB	Decibel
PM	Phase Margin
GM	Gain Margin
BJT	Bipolar Junction Transistor

Chapter1:

Introduction

1. Motivation

Opamp plays an important and fundamental role in analog and mixed signal circuits and systems. Precision opamps previously used in instrumentation are now-a-days being used in industrial and automotive applications. Hence,there always exists a need for better precision opamps. The auto zero amplifiers provide the lowest offset and offset drift over temperature and time with low power. But,it is a discrete system. In analog systems, we need to have a continuous output. Hence, an improved yet simple architecture is required to replace auto zero amplifiers. Another aspect is that the design should be able to perform correctly in extreme environments. It should operate under a wide temperature range. The highlighted target features of this design are less than 50 μV offset voltage, 0.1 μV/°C offset voltage drift, and 1 mW power consumption.

2. Thesis organisation

This thesis provides a two and forth action opamp capable of producing continuous output with very low (≤15uV) offset voltage. Chapter 2 describes the basic two stage classical opamp. The different parameters associated with an opamp are explained.Also, the difference between real and practical opamp is explained. Chapter 3 describes the offset voltage of an opamp, it's causes and it's different cancellation techniques. Chapter 4 describes the ping pong auto zero architecture. The different components and their importance are explained. Finally; chapter 5 provides all the simulation results. All the layouts are shown in the Appendix.

Chapter2:

Basic Opamp

1. Differential Amplifier

Differential amplifier is one of the most important circuit in analog domain. As it's name suggests it only processes the difference between the two input signals. It cancels out the common voltage applied to both inputs. But, practically there always exists some amount of common voltage both at the inputs. As, it cancels most of the common voltage at the input hence, noise and bias voltages are cancelled out. Most of the electronic circuits use differential amplifiers.

The output of the differential amplifier is given by,

$$V_{out} = A_d(V_{in+} - V_{in-}) + A_c((V_{in+} + V_{in-})/2)$$

Ideally,

$A_c=0$

Where A_c is the common mode gain of the amplifier and A_d is the differential mode gain of the amplifier.

When using a differential amplifier it is desirable to null out noise and bias voltages that appear on both inputs so a low common-mode gain is usually considered good. The common-mode rejection ratio is usually defined as the ratio between differential-mode gain and common-mode gain and it characterizes the efficiency of the amplifier in refusing voltages that are common to both inputs from affecting the output. Common-mode rejection ratio (CMRR) is given by:

$$CMRR=A_d/A_c$$

For an ideal differential amplifier A_c should be zero and CMRR should be infinite.

A differential amplifier must have two inputs and one or two output terminals. Generally, it is used as the input stage of many analog circuits, as it has high differential gain, very high input impedance , also low output impedance and high noise cancellation.

The gain of the differential amplifier is given by,

$A_V = - g_m R_D$

Where g_m is the transconductance of the input differential pair.

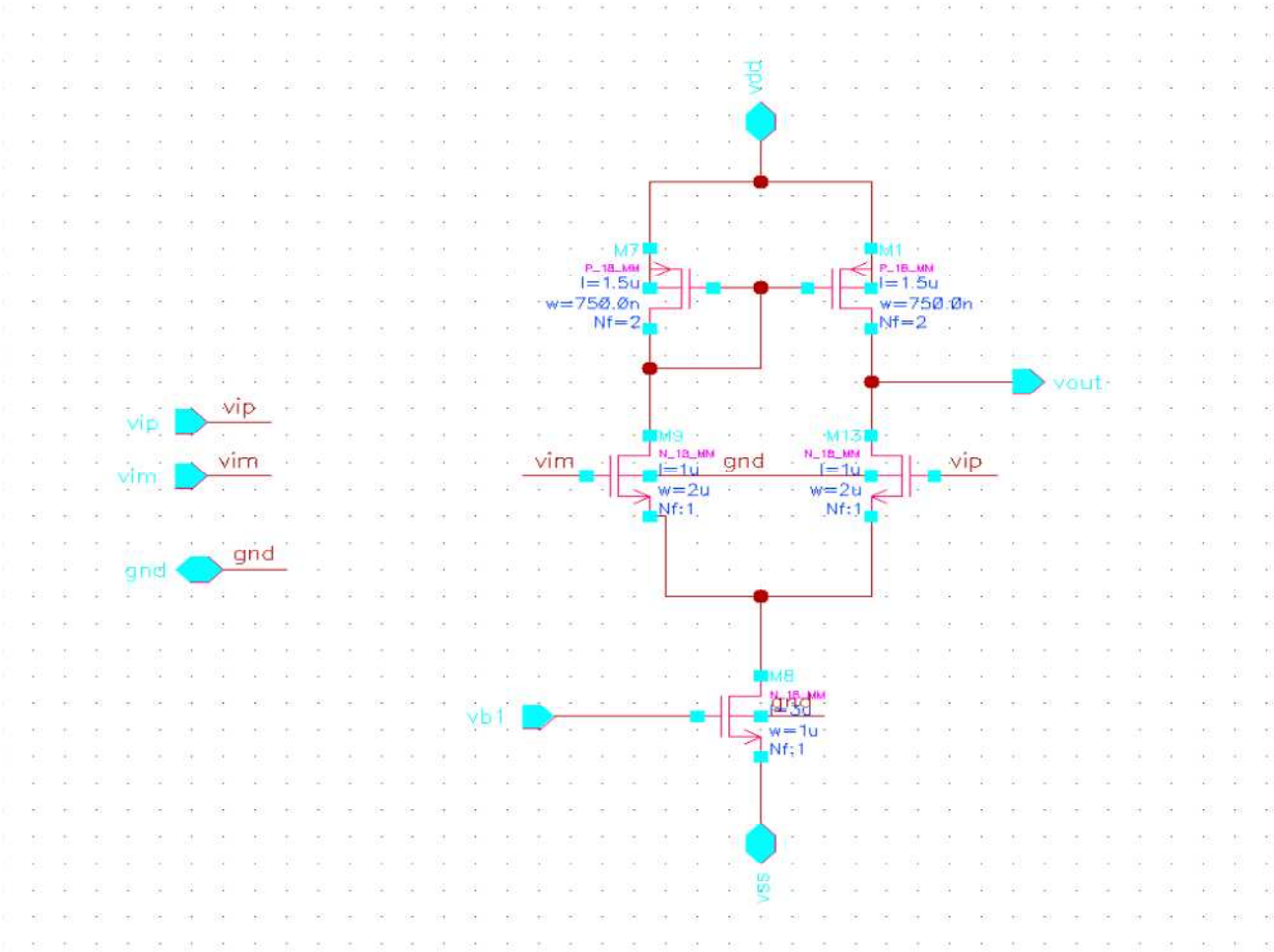

Fig 1: Differential Amplifier Schematic.

It is the main block in the opamp circuit. The opamp's performance mainly depends upon this circuit.

The opamp circuit generally consists of three levels as indicated in the figure below.

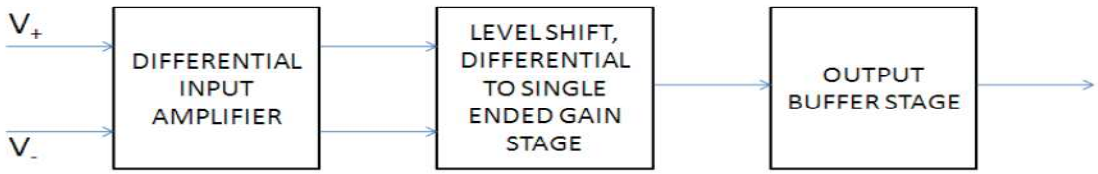

Fig 2: Block diagram of a general opamp.

The output buffer stage helps increase in the output swing of the opamp. It also provides the adequate gain to the opamp.

2. Ideal and Practical Opamps

Ideal opamps often considered as the theoretical opamps are the best ever achievable practical opamps. But, it is very hard to achieve the specifications of an ideal opamp in real environment. Many real life constrains make it impossible to achieve such results.

Table 1: Ideal and practical opamp comparison

IDEAL OPAMP	*PRACTICAL OPAMP*
R_{IN} = infinite	$R_{IN} \neq$ infinite (in terms of MOhms)
R_{OUT}=zero	$R_{OUT} \neq$zero (in terms of KOhms)
GAIN = infinite	GAIN ≠ infinite (in order of 10000)
CMRR = infinite	CMRR ≠ infinite(very high)
PSRR = infinite	PSRR ≠ infinite (very high)
OFFSET = zero	OFFSET ≠ zero (in order of milivolts)
SLEW RATE = infinite	SLEW RATE ≠ infinite(in order of 10 V/us)

Here, offset is considered as output offset voltage.

3. Different Parameters of Opamp

An opamp has different parameters associated with it, which affects very much it's performance. These parameters need to be understood. The parameters are given as below:

ICMR: Any practical opamp has an input as well as output range. It is defined as the maximum common mode input voltage up to which the transistors in the differential stage (first stage) are in saturation.

CMRR:It is defined as the ratio of differential mode gain value to the common mode gain value. An ideal opamp should have very high CMRR value, as it is one of the most important basic parameter of the opamp. It is often measured in dB.

PSRR: It indicates how well the opamp acts to the variation of power supply(both positive and negative supply). More is the variation of output of opamp corresponding to the variation of power supply, lesser is the PSRR.An opamp should have very high PSRR.It is often measured in dB.

Output Range: It is defined as the range of the opamp output. It should be nearly equal to twice of the magnitude of the power supply.

Slew Rate: It is defined as the maximum time rate of change of output. It is a small signal phenomena unlike settling time, which is a large signal phenomena. It is expressed in V/us. An good opamp should have high slew rate.

Phase Margin: It is defined as the amount of phase need to be added to make the system marginally stable at the gain cross over frequency. It is measured at the point where system gain is 0 dB.

$$PM = 180+Ó$$

Ó = Phase of system when gain is 0 dB.

Gain Margin: It is defined as the amount of gain need to be added (in dB) to make the system marginally stable at the phase cross over frequency. It is measured at the point where system phase is 180^0.

$$GM = 20 \log (1/Av)$$

Av = Gain of system when phase is 180^0

Both phase margin and gain margin need to be positive for the opamp to be stable.However, phase margin is more important parameter, as it also affects the transient response such as the settling time, overshoot.(Larger is the PM lesser is the overshoot)

4. Opamp uses and applications

Opmap has got many applications in analog and digital domain. But, we take a look at some of the basic yet important applications of opamp in analog field.

Summing Amplifier (Adder): The summing amplifier is a handy circuit enabling to add several signals together. The summing action of the circuit shown in Figure 2 is easy to understand. By keeping the negative terminal close to 0V (virtual ground) the op-amp essentially nails one leg of R1, R2 and R3 to a 0V potential. This makes it easy to write the currents in these resistors.

I1 = V1 / R1; I2 = V2 / R2; I3 = V3 / R3

According to Kirchhoff's law, we get I = I1 + I2 + I3 and

V0 = - RF (V1 / R1 + V2 / R2 + V3 / R3)

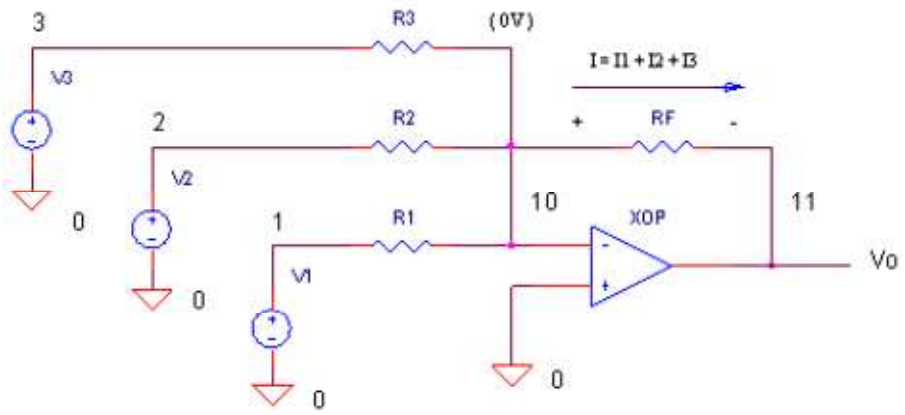

Fig 3: Summing Amplifier.

Differential Amplifier: The difference op-amp produces the algebraic difference between two input voltages, which is shown in Figure 3. When RF=Rin and RA=RB the output of the amplifier can be given as VO= (□A/RF) (VA - VB). Thus the setup amplifies the difference of two voltages by a constant gain set by the used resistances.

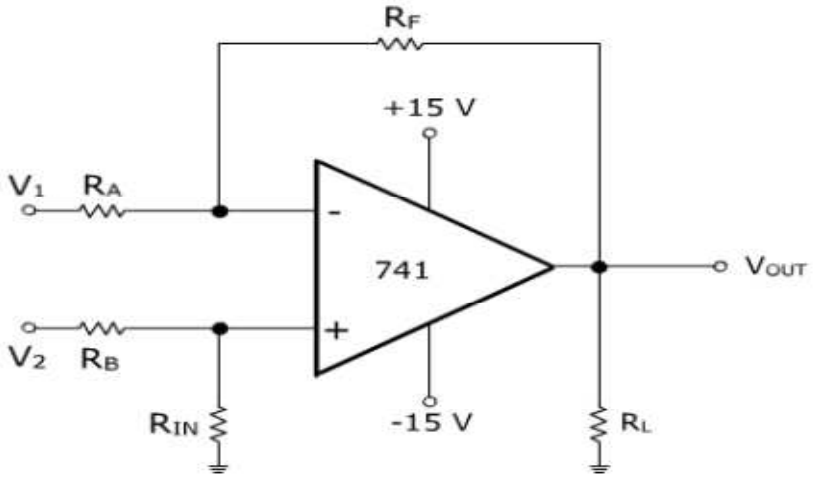

Fig 4: Difference Amplifier.

Log and Antilog Amplifiers: In analog compression processes, log amplifiers are used. Log amplifiers use diode or bjt in the feedback path. Antilog amplifier operation is just is the opposite operation (expansion).

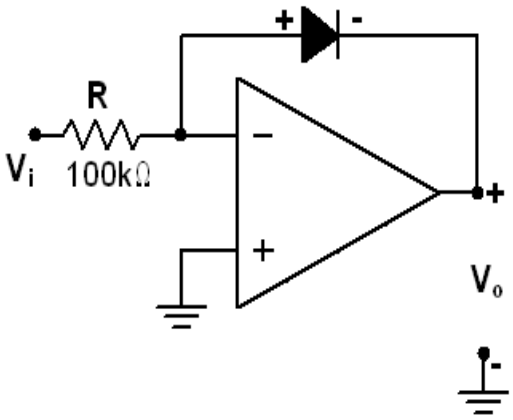

Fig 5: Log amplifier using diode.

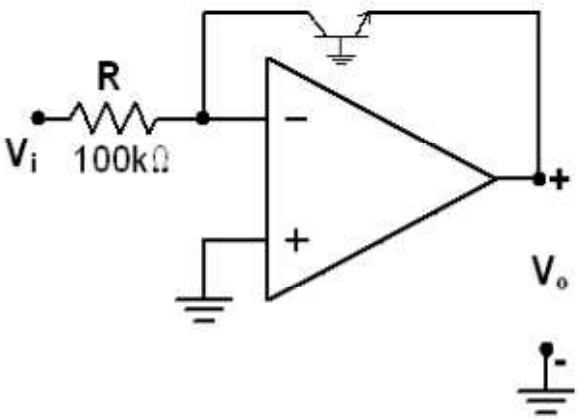

Fig 6: AntiLog amplifier using BJT.

The output voltage of log amplifier is given by,

$$V_0 = - V_T \ln(Vi/RI_o)$$

Where $V_T = kT/q$

I_0 = diode current

(k = boltzman constant)

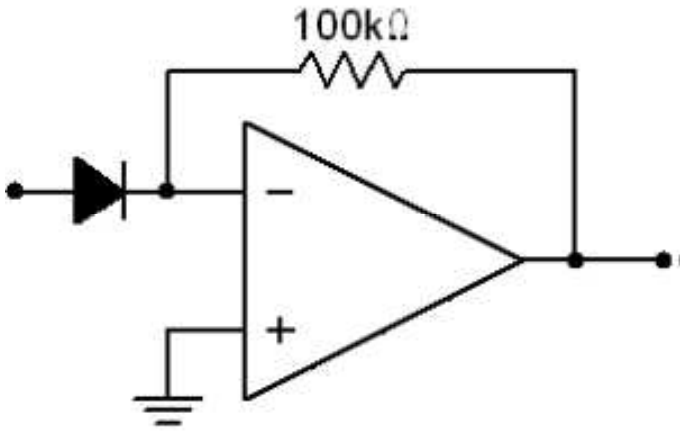

Fig 7: Antilog amplifier.

Chapter3:

Offset Voltage of Opamp

1.Introduction

The input offset voltage can be defined as the voltage, which is applied between the two input terminals of the opamp to obtain zero volts at the output. The input offset voltage can be either positive or negative in polarity.It can be in the order of micro to mili volts.Generally, bjt opamps will have lesser offset voltage than cmos opamp. The circuit showing the input offset voltage connected in series with the negative terminal of the opamp is shown below.

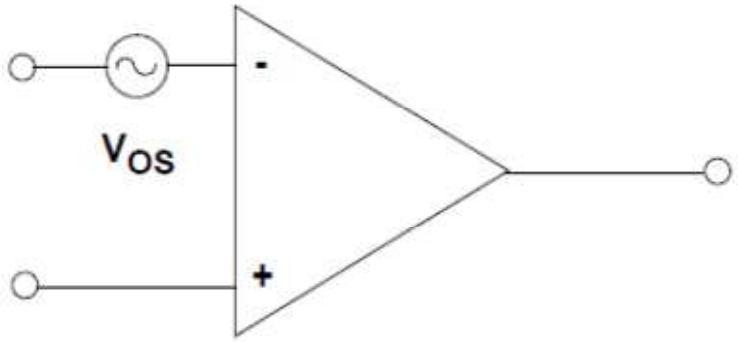

Fig 8:Opamp with input offset voltage

The offset voltage can be connected to any of the input i.e either positive or negative.The offset voltage also varies with temperature and aging.

The relation between offset voltage and temperature is given by,

$$V_{off}TC = \Delta V_{off}/\Delta T$$

For $V_{off}TC = 25uV/^0C$, The drift is (over a temp. range = 10^0C):

$$\Delta V_{off} = V_{off}TC \times \Delta T$$
$$\Delta V_{off} = 25 \times 10$$
$$= 25 \text{ mV}$$

The offset voltage also changes with aging or time. It is generally measured in uV/month or uV/1000 hours. Generally, it is measured for the first 30days of operation.

For different device processes, the offset as well as it's drift vs time and temperature varies accordingly. It is shown in the below table.

Table 2 : Range of Input Offset voltage and drift for different device processes

PROCESS AND DEVICE TYPE	V_{IO}^{max} at 25°C (µV)	ΔVIO/ΔT† (µV/°C)	VIO Full Range (µV)	Long term Drift† (µV/month)
Bipolar	150 – 10000	1 – 10	240 – 15000	
LM324	7000		9000	
TLE2021	500	2	750	0.005
THS4001	8000	10	10000	
BiFET	800 – 15000	1 - 30	3000 - 20000	
LF353	10000	10	13000	
TLE2071	4000	3.2	6000	
TL051	3500	8	4500	0.04
CMOS	200 – 10000	<1 – 10	300 - 13000	
TLC071	1000	1.2	1500	
TLV2471	2200	0.4	2400	
TLC2201	200	0.5	300	0.005

2.Causes of Offset in Opamp

The cause of input offset voltage is due to the inherent mismatch of input transistors & components during silicon die fabrication and stresses retained on the die during the packaging process (minor contribution). These effects collectively generate a mismatch of the bias currents which flows through the input circuit & primarily the input devices; resulting in a voltage differential at input terminals of the opamp. VIO has been reduced with modern manufacturing processes through increased matching & improved package materials and assembly.

Typically, most opamps consists of a differential-pair amplifier as the input stage. A simplified version is shown in Figure 9, where Q1 (+ or noninverting input terminal) and Q2 (– or inverting input terminal) are MOS transistors. The input terminals of the opamp are gates of these transistors. The current source biases the transistors and each leg of the circuit is balanced so that one half of the current flows through each transistor ($IQ_1 = IQ_2 = I_{DC}/2$) and the inverting & noninverting inputs are at the same potential. Mismatches in R, Q_1, and Q_2 unbalance this current. The gate voltages of the transistors then become unequal, creating the small differential voltage, V_{IO}.

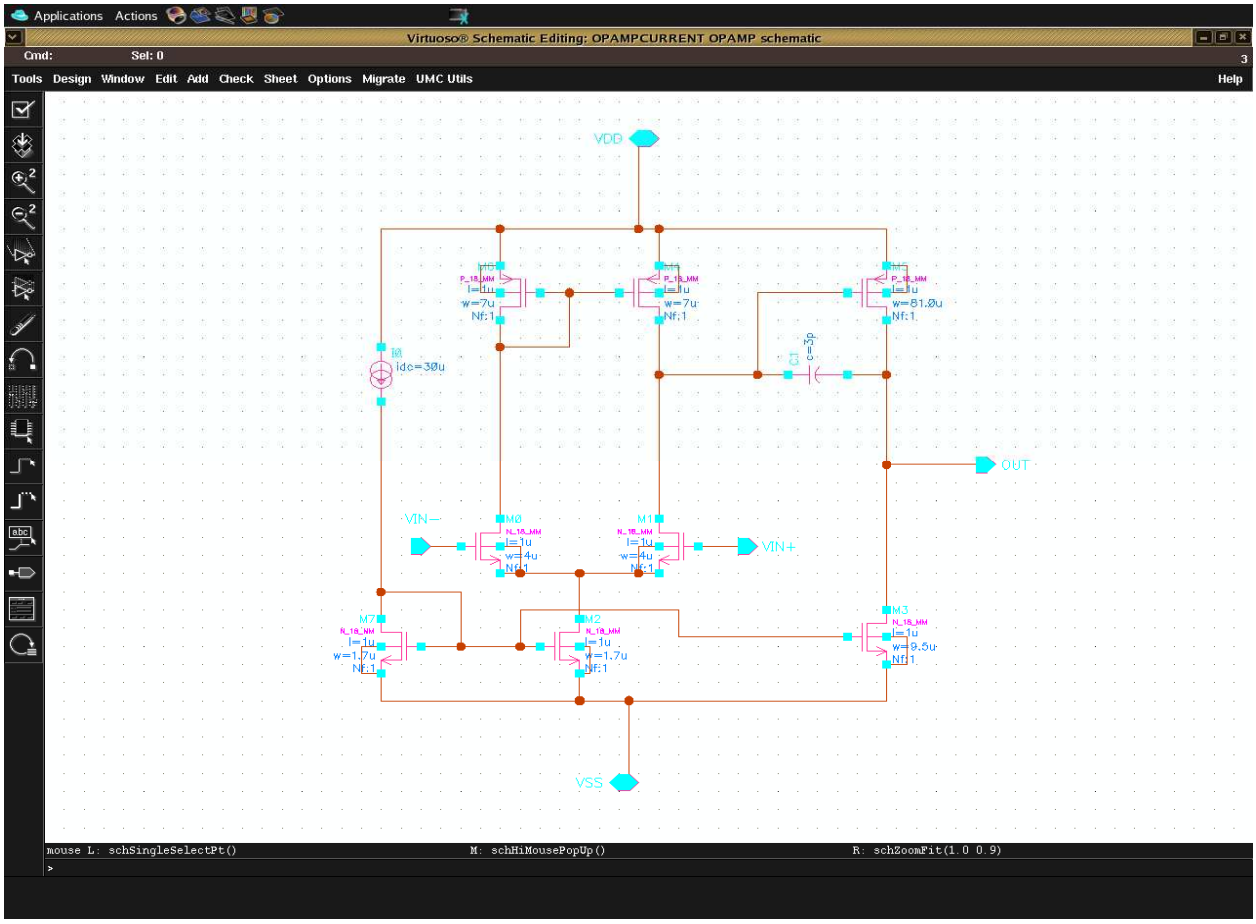

Fig 9 : Opamp Schematic.

The offset can be catagorised into two parts, i.e random and systematic. Systematic offset causes due to channel length modulation of transistors. It arises due to the nonlinear operating chracteristics of the devices or due to the influence of parasitic in the device path or signal path. On the other hand, random offset causes due to variations of physical parametres of the transistors after fabrication. This is the result of the stochastic nature of many physical processes. The stochastic nature of the charge carriers of a conductor results in various types of noise signals. During fabrication process, the stochastic nature of the physical phenomena causes random variation of the fabricated chip and mismatches between same size transistors.

3. Methods of Offset Cancellation

There has been many methods found for the effective offset cancellation. Basically,it can be divided into two catagories as chopper and autozero technique.

3.1.Chopper Amplifier

The chopper amplifier was invented more than 50 years ago.It was very popular in those days.Often, it has been wrongly interpreted as chopper stabilised amplifier or autozero amplifier. It provided very low offset voltage and offset drift. But it's bandwidth was limited to few KHz, which adversly affected the ac performance.

Following is the diagram of a chopper amplifier operating in frequency domain.

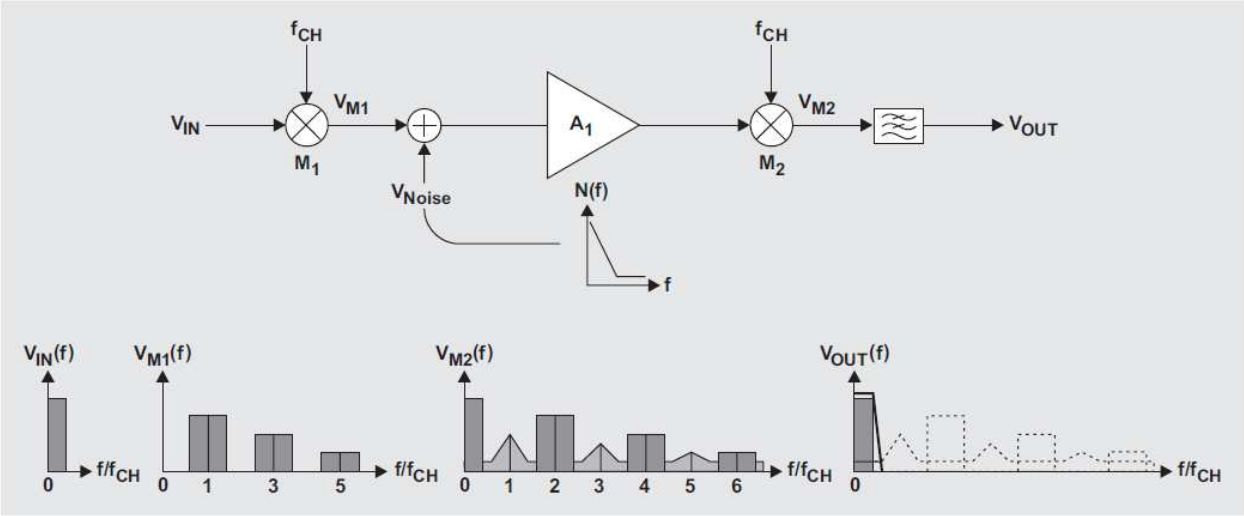

Fig 10: Chopper Amplifier operating in frequency domain.

As shown in the above figure, the input to the amplifier is a low bandwidth signal. It is being fed to the switch (in time domain), which acts here as a frequency(AM) modulator. As, the clock driving the switch is a square wave, hence in frequency domain it will have only odd harmonics with amplitude decreasing with the value of n (n indicates nth harmonic).The square wave modulates the input signal resulting in $V_{M1}(f)$. Now, as a natural process low frequency noise and dc offset gets added. The low frequency noise also known as the 1/f noise is having the fourier spectrum N(f). Now, when the noise additive signal passses through 2^{nd} switch, It again gets modulated. Actually, the signal gets demodulated and the noise gets modulated. Now, the spectrum $V_{M2}(f)$ results.As we can see, the 1/f noise and dc offset is having very less amplitude in the signal frequency domain. It is now filtered out by passing through a low pass

filter having the cut-off frequency same as the signal bandwidth. Hence, finally the effect of the 1/f noise and dc offset gets nullified to a great extent. But, the signal frequency must be much less than the carrier (switch) frequency for the proper operation. It has the drawback of having low bandwidth.

3.2.Chopper Stabilised Amplifier

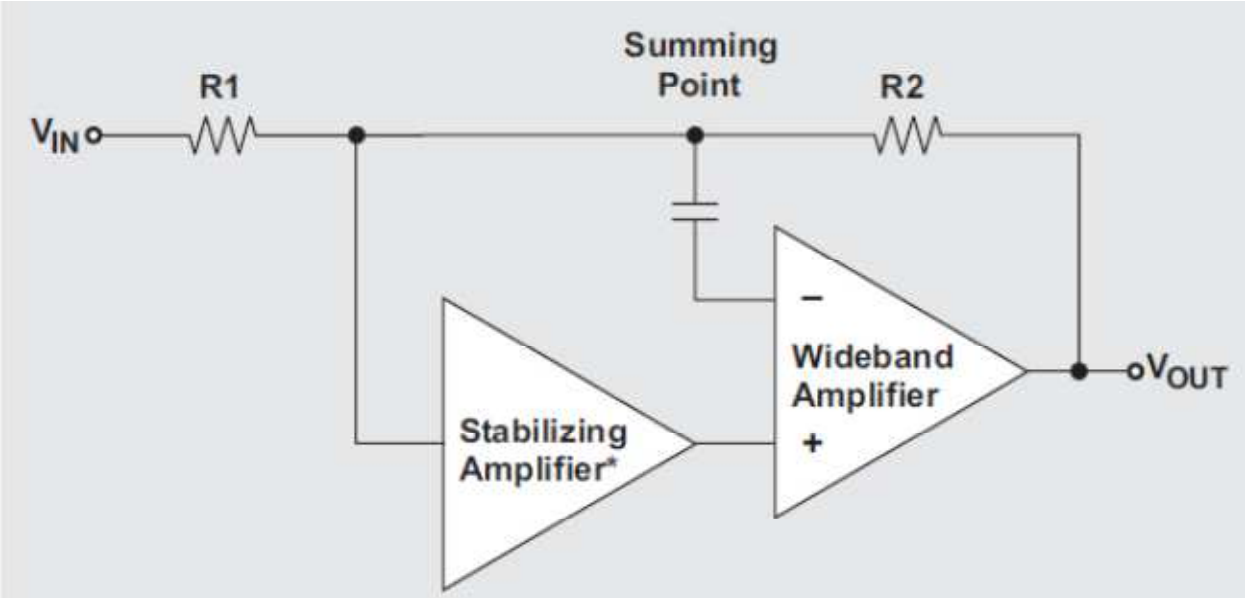

Fig 11: Chopper stabilised amplifier.

The chopper stabilised amplifier solves the low bandwidth problem of the chopper amplifier. But, It comes with another problem of having only the inverting terminal for signal processing. Also, the cost and complexity increases.

3.3.AutoZero Amplifier

The autozero amplifier eliminates both the short comings of chopper as well as chopper stabilised amplifier. It uses an auxiliary input port in addition to the basic input port for the offset cancellation. It uses the main input port for signal processing while cancelling the offset using the auxiliary input. To do this operation, it nedds two phases, i.e sampling and amplifing. It is clear that the same amplifier cannot process signal and cancel offset simultanously.

Hence, It becomes a discrete phenomena. Yet, it provides very good offset cancelling with both terminals being used. Here, the offset cancellation means it can cancel a good amount of offset in order of 5-10 milivolts being put at the input port.

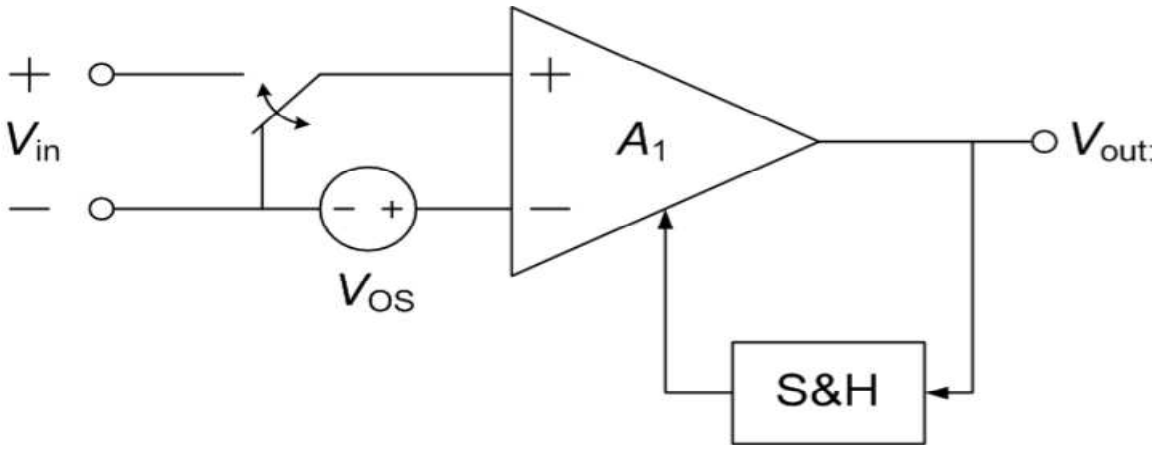

Fig12: AutozeroTechnique.

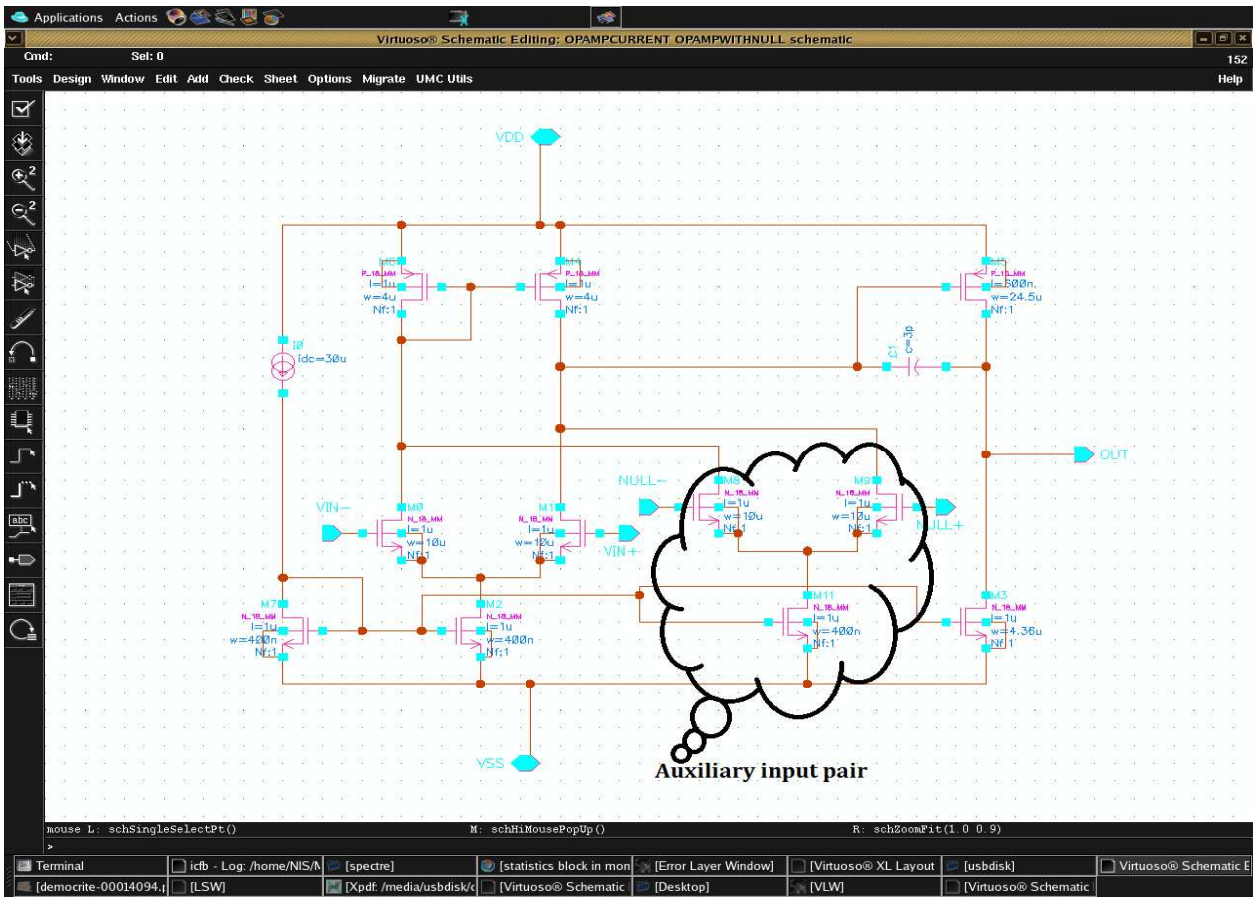

Fig 13: Addition of auxiliary input port for autozero operation.

Chapter 4:

Ping Pong Auto zero Architecture

1. Introduction

The name ping pong implies two and forth action. It consists of two identical amplifiers, switch, sample and hold circuit and switch driver. The need of this architecture arises from the problem that auto zero amplifier cannot alone produce continuous output. As we recall from chapter 3, auto zero amplifiers operate in two phases. During one phase, amplification and during another sampling is done. Hence, it cannot produce continuous output. The ping pong on the other hand employs two auto zero identical amplifiers such that either one of them always processes the input signal, hence producing a continuous output. Also,at the same time either one of them does the offset cancellation making it also continuous. Finally, we get a offset free continuous output.

The ping pong auto zero block diagram is shown below:

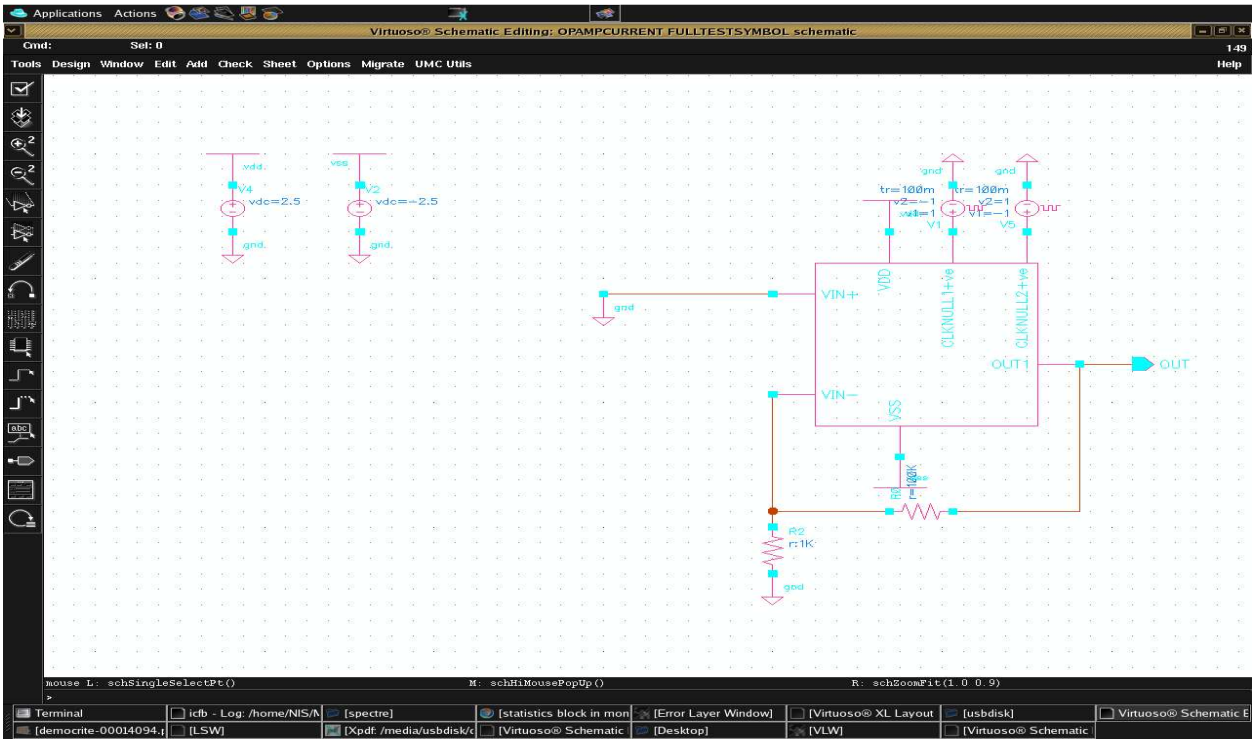

Fig 14: Ping-Pong auto zero opomp block diagram.

As we see in the above figure, the opamp as usual consists of two inputs Vin+ and Vin-, along with V_{DD} and V_{SS} dual power supply. It consists of two external clock inputs also. These two clock drive the two phases and must be of same period and opposite polarity.

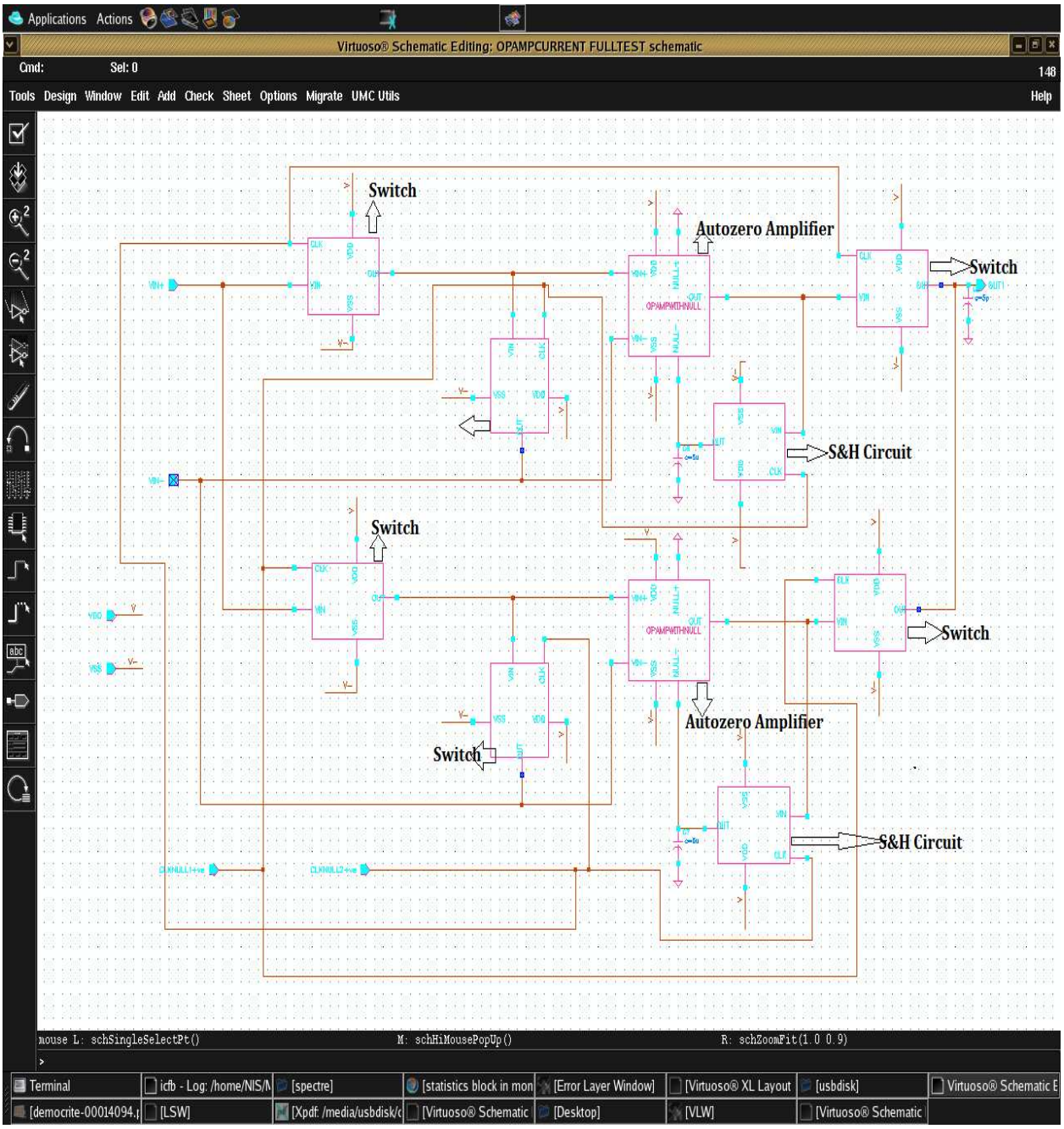

Fig 15: Inner Blocks Of Ping-Pong auto zero opamp.

2. Components of Ping-Pong Architecture

2.1. Opamp employing Auto zero

An auxiliary input pair is added to the classical two stage opamp in order to make it auto zero amplifier. Two such identical amplifiers are needed for the ping pong architecture. The gain of the basic opamp is divided into 2 equal parts i.e. Av becomes Av/2 for both input as well as auxiliary input pair. Hence,now the gain of the auto zero amplifier becomes Av/2 in comparison to gain of basic Opamp which is Av. Also the gains of main and auxiliary input pairs becomes equal. The schematic is same as shown in Fig 13.

2.2. Sample and Hold Circuit

The sample and hold circuit is the most important circuit as per the accuracy of the design. The work of the sample and hold circuit is to sample the input offset voltage during the sampling phase and then to hold it during the amplification phase. So,the offset gets cancelled during the amplification phase. Hence,we get an offset free amplification of the input signal.

The sample and hold circuit can be built by using a nmos in series with capacitor. This is the simplest sample and hold circuit. But, the problem with this circuit is "charge injection effect", which makes it not suitable for this design. This design needs a highly accurate S&H circuit.

Charge injection Effect: During the on or conduction phase, a channel develops between the oxide and silicon interface. This channel (acts as capacitor) stores some charge during the on phase. When the nmos becomes off, the stored charge gets shared between the input source and the holding capacitor. When the charge gets injected into the capacitor, the output becomes erroneous.

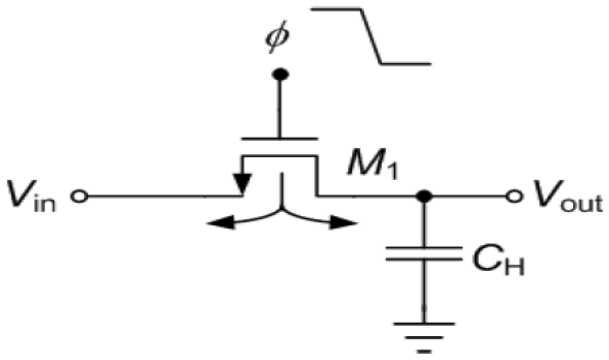

Fig 16: Simple sampling circuit.

The charge stored is given by,

$$Q_{st} = WLC_{OX}(V_{DD} - V_{IN} - V_{th})$$

The residual voltage on the capacitor during off state is given by,

$$\Delta V = (WLC_{OX}(V_{DD} - V_{IN} - V_{th}))/C_H$$

There is also another undesirable effect associated with the above sampling circuit. It is known as clock feed through effect.

Clock feed through Effect*:* During the high to low transition of the clock signal the gate-drain and gate-source overlap capacitance along with holding capacitance form a path between clock input and ground. Hence,a voltage divider circuit is formed between clock and output. It creates an error in the output value.

The residual or erroneous voltage across C_H is given by,

$$\Delta V = V_{clk}\, C_{gd}/(C_{gd} + C_H)$$

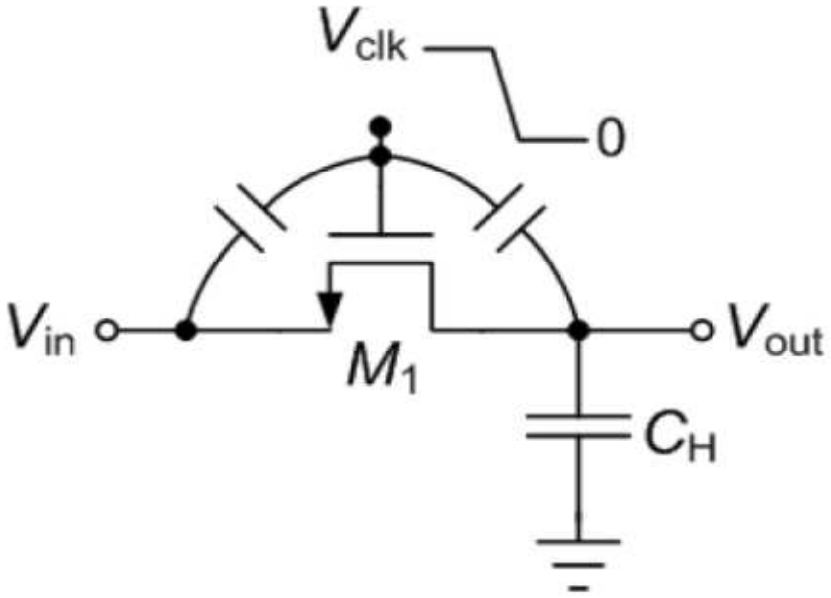

Fig 17: Clock feed through effect.

However, by increasing value of C_H and decreasing value of W/L ratio both the effects can be compensated to some extent.

Complementary switch and dummy switch are the two approaches adopted in this project for reducing the above two effects. Complementary switch is structure containing a nmos connected to a pmos as shown in the Fig 18.

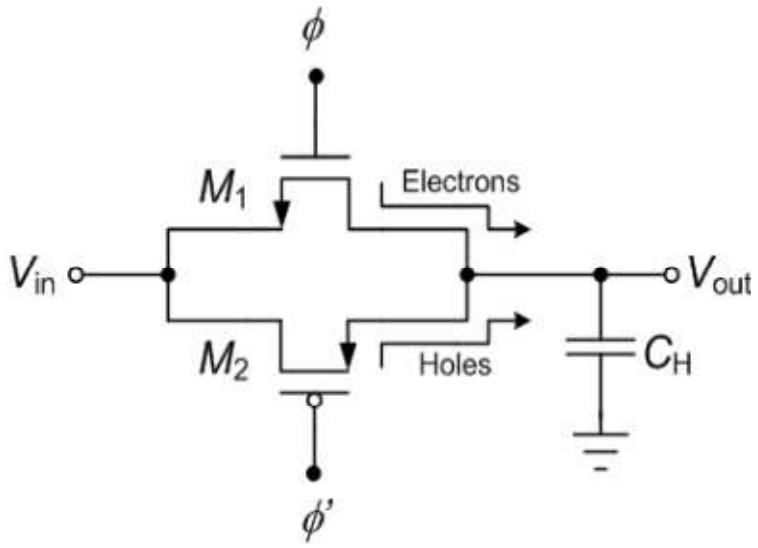

Fig 18: Complementary Switch.

Here, as the charge carried by nmos is opposite in polarity to charge carried by pmos, the charge injected by the nmos will be cancelled during the off phase by pmos. But, both the charges magnitude must be same. Unfortunatly, the gate drain overlap capacitance is not same in nmos and pmos. Therefore, this mechanism cannot cancel the charge injection completely. Reduction of on resistance is one of it's additional advantage. On the other hand, dummy switches can also be employed to reduce the errors.

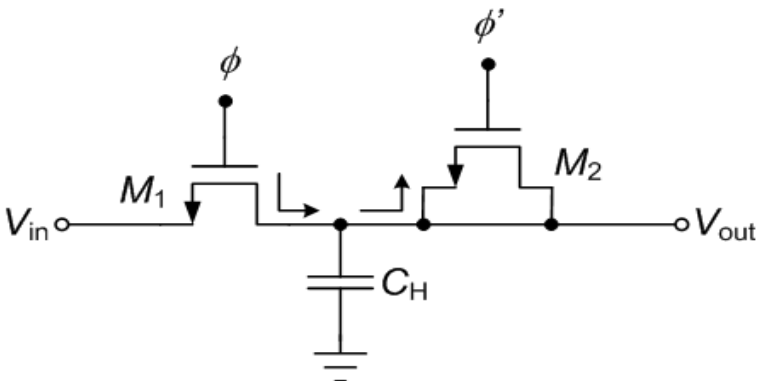

Fig 19: Dummy switch.

As shown in the above figure, during the off phase (M1 is off and M2 is on) the charge injected from M1 finds way through M2 , as M2 is on and there is a formation of channel between gate to source of M2.This channel absorbs the charge injected from M1.Similarly,when M1 is on and M2 is off, the charge injected from M2 finds way through M1 to the low

impedance input signal. Hence, the output remains error free. For proper operation, there should be no delay between the Ǿ and Ǿ'.

To get a even better solution, both the mechanisms are combined as shown in the below figure.

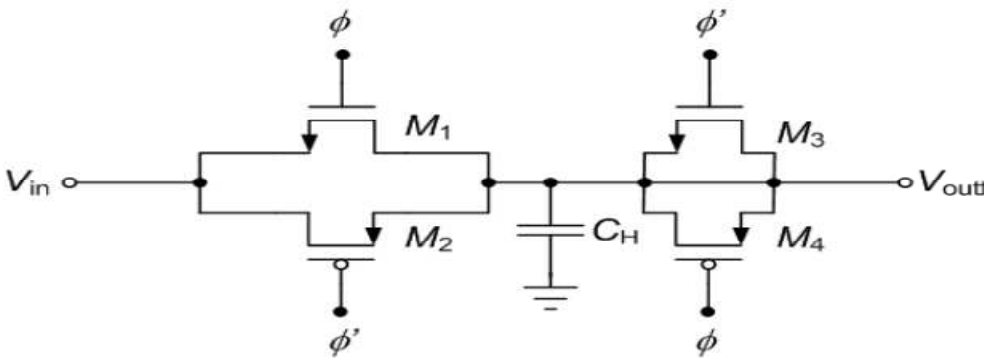

Fig 20: Complementary switches with dummy switches.

In this project, $C_H = 5u$

$(W/L)_1 = 10$

$(W/L)_2 = 4$

$(W/L)_3 = (W/L)_4 = 0.5$

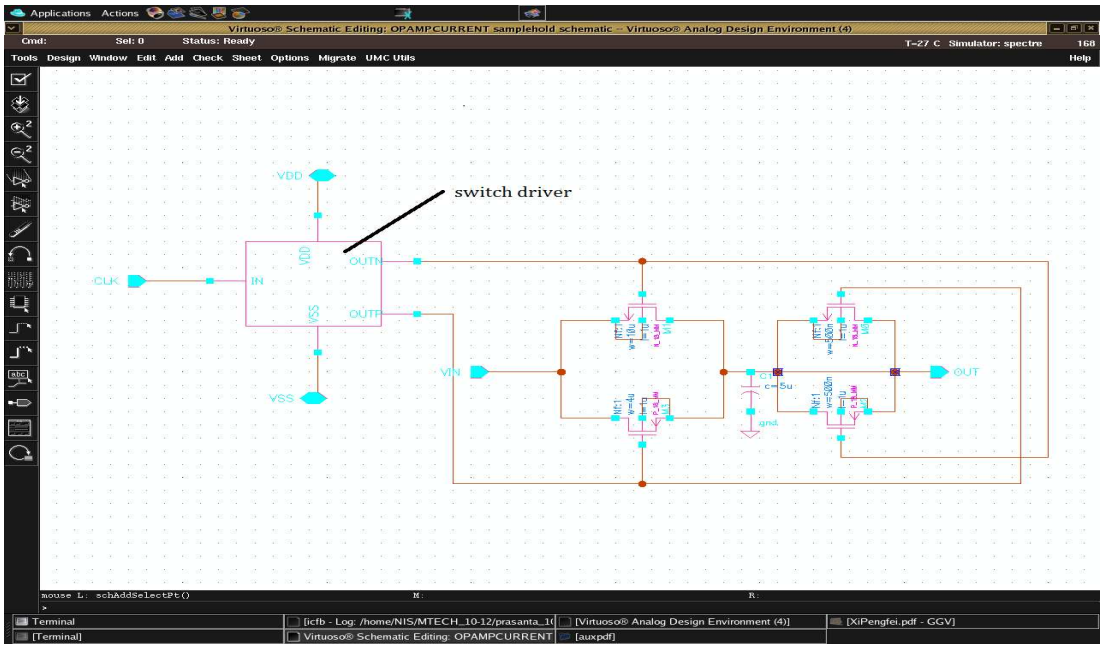

Fig 21: Sample and hold circuit with switch driver.

2.3. Switch and Switch Driver

Simply using an inverter may damage the very purpose of the above sample and hold circuit. The need of simultaneous on and off of the M1, M2 and M3,M4 transistors respectively gives rise to clock driver. It generates two overlapping signals and provides low clock skew between the two signals.

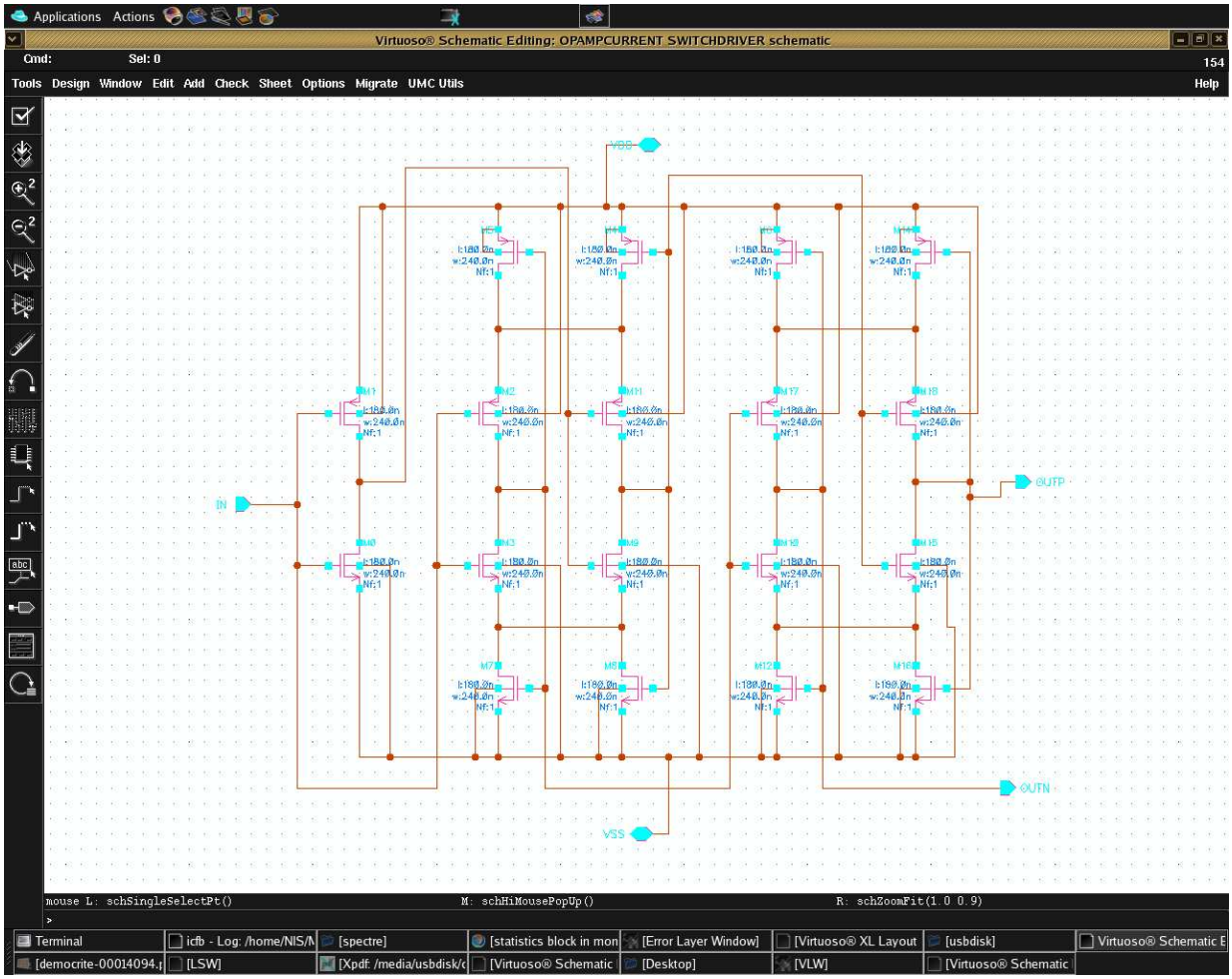

Fig 22: Switch Driver Schematic.

In this project, cmos transmission gate is used as the switch with (W/L) of nmos set as 10 and (W/L) of pmos set as 4.

Chapter5:

Simulation and Results

1. Different Parameters Of Basic OPAMP

The basic opamp has been designed as per a certain design procedure as given in Allen Holberg [15]. A two stage classical approach has been adopted. The design has been with regard to the set of specifications mentioned below.

Boundary Conditions Requirement

Table 3: Boundary conditions of basic opamp.

Supply Voltage	±2.5
Temprature Range	0 – 70° C

Specifications

Table 4: Specifications of basic opamp.

Gain	70dB
Gain Bandwidth	5Mhz
Phase Margin	60°
Slew Rate	10V/us
Input Common Mode Range	-1 ~ 2
CMRR	60dB
PSRR	60dB
Offset	10mV
Power Dissipiation	2mW
Output Swing	-2 ~2

Different equations governing the above parameters have been followed. They are listed below.

Slew rate = I_5/C_c

Gain Bandwidth = g_{m1}/ C_c

Positive CMR = Vin (max) = $V_{DD} - (I_5/ß_3)^{0.5} - \square V_{T03}(max)\square + V_{T1}(min)$

Negative CMR = Vin (min) = $V_{SS} + (I_5/ß_1)^{0.5} + V_{T1}(max) + V_{DS5}(sat)$

Saturation voltage $V_{DS} = (2I_{DS}/ß)$

Gain = $2(g_{m2})(g_{m6})/(I_5I_6(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7))$

Here, I_5 = 30uA and C_c = 3pF

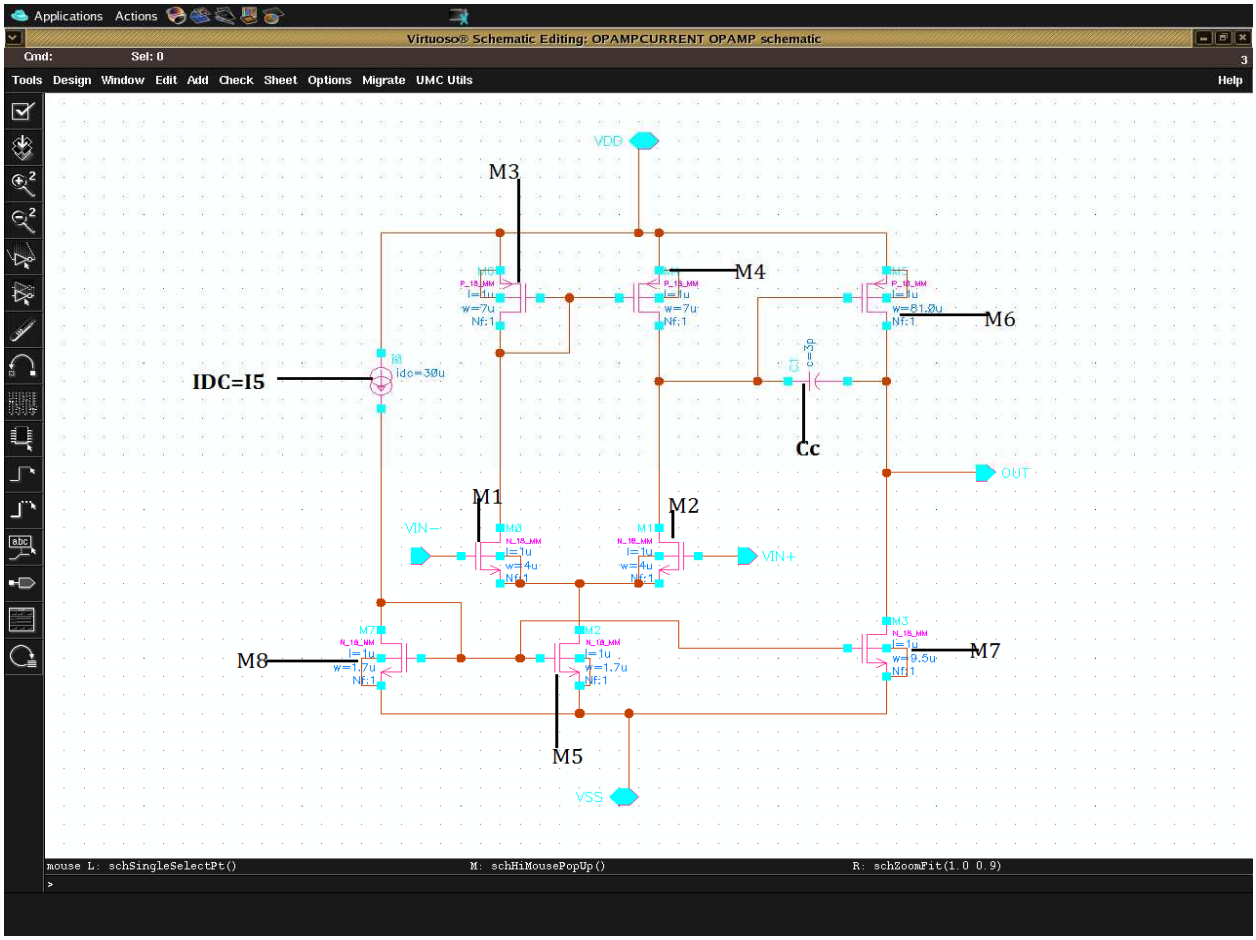

Fig 23: Basic opamp schematic with labeling.

According to the design procedure (equations) sizes of the transistors have been determined.

Table 5: transistor sizes of basic opamp

$(W/L)_1$	4
$(W/L)_2$	4
$(W/L)_3$	7
$(W/L)_4$	7
$(W/L)_5$	1.7
$(W/L)_6$	81
$(W/L)_7$	9.5
$(W/L)_8$	1.7

Following are the results obtained through simulation.

Table 6: basic opamp simulation results

Gain	75dB	
Gain Bandwidth	8.6Mhz	
Phase Margin	66.7^0	
Slew Rate	9.9V/us	
Input Common Mode Range	-1.54 ~ 2.15	
CMRR	78.5dB	
PSRR	82.5dB(+)	111.1dB(-)
Offset	-51.755uV	
Power Dissipiation	1.125mW	
Output Range	-2.42~2.48	

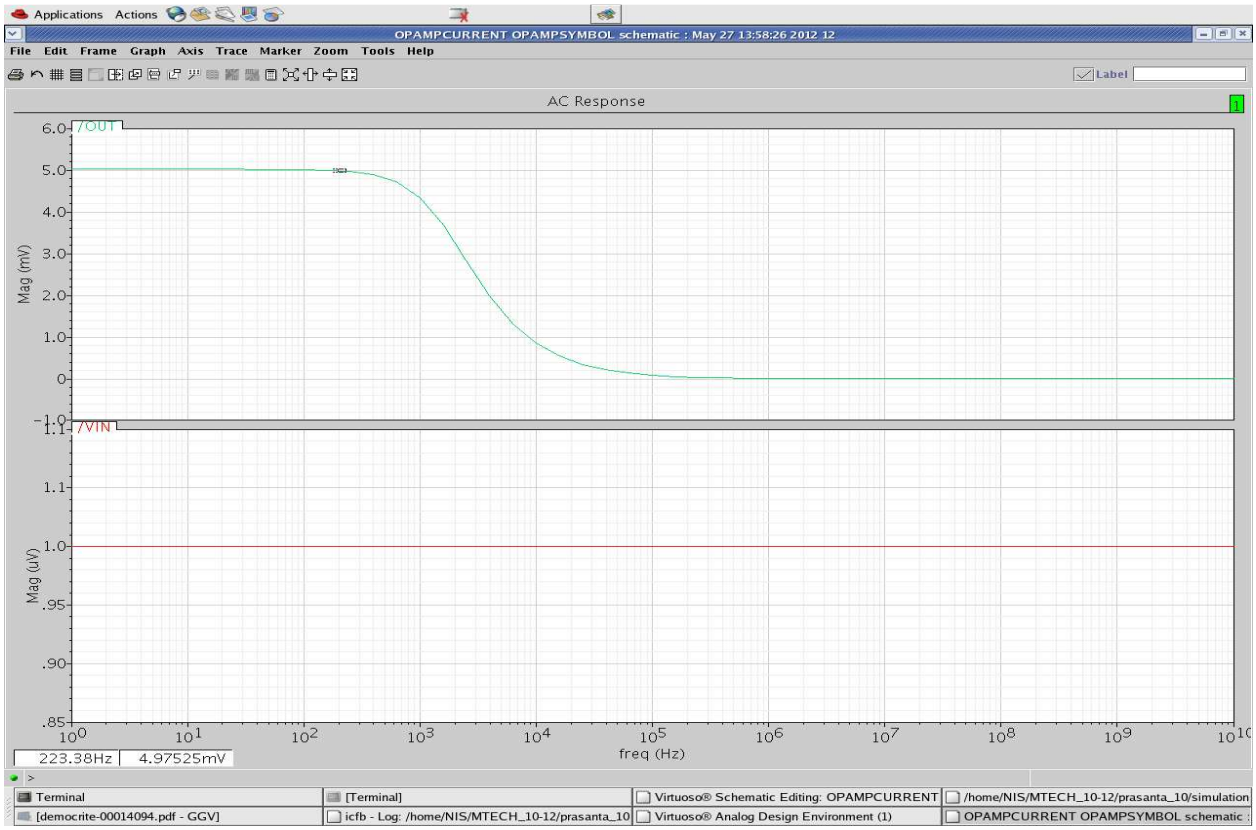

Fig 24: Gain of basic opamp.

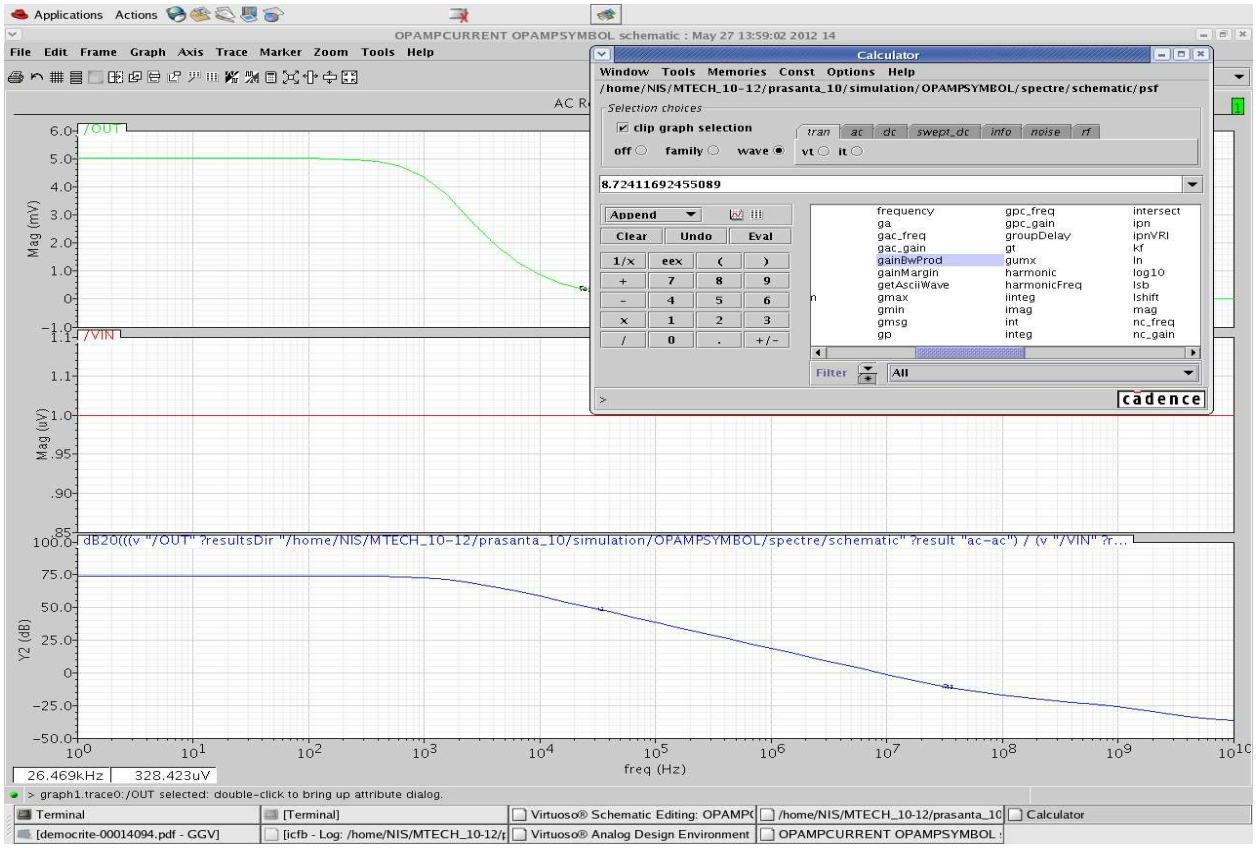

Fig 25: UGB of basic opamp.

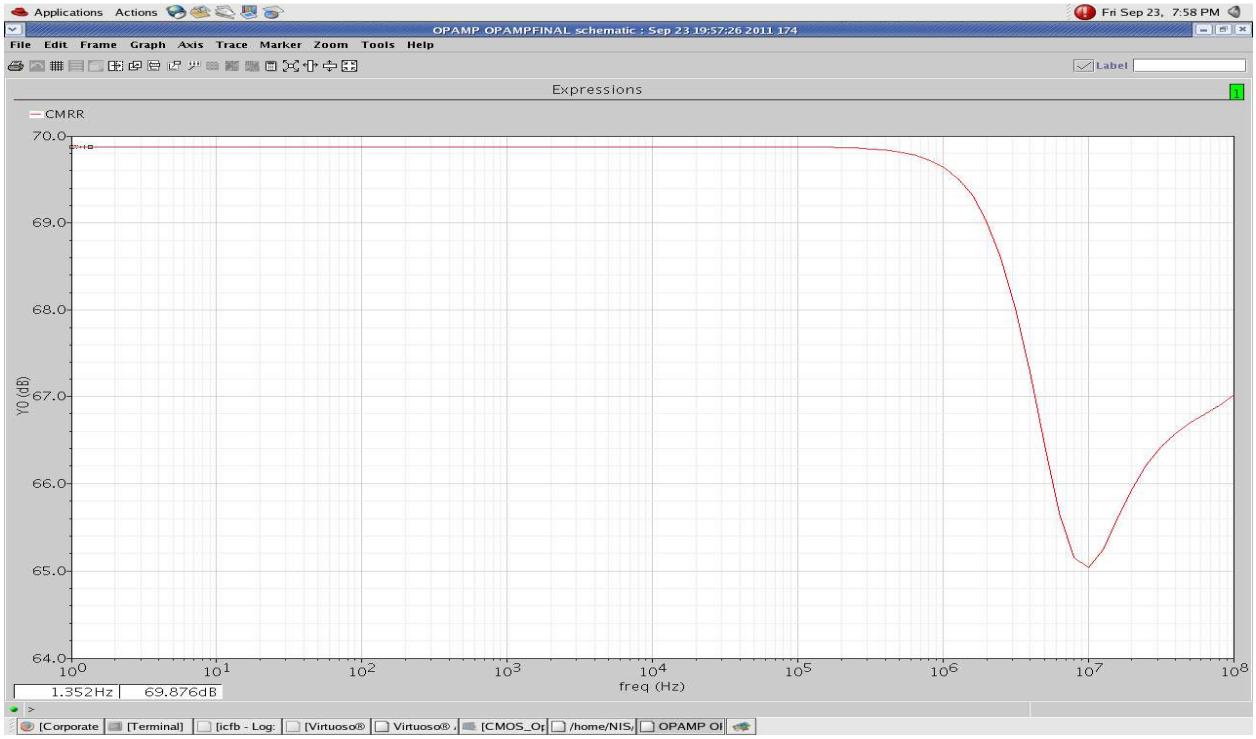

Fig 26: CMRR of basic opamp.

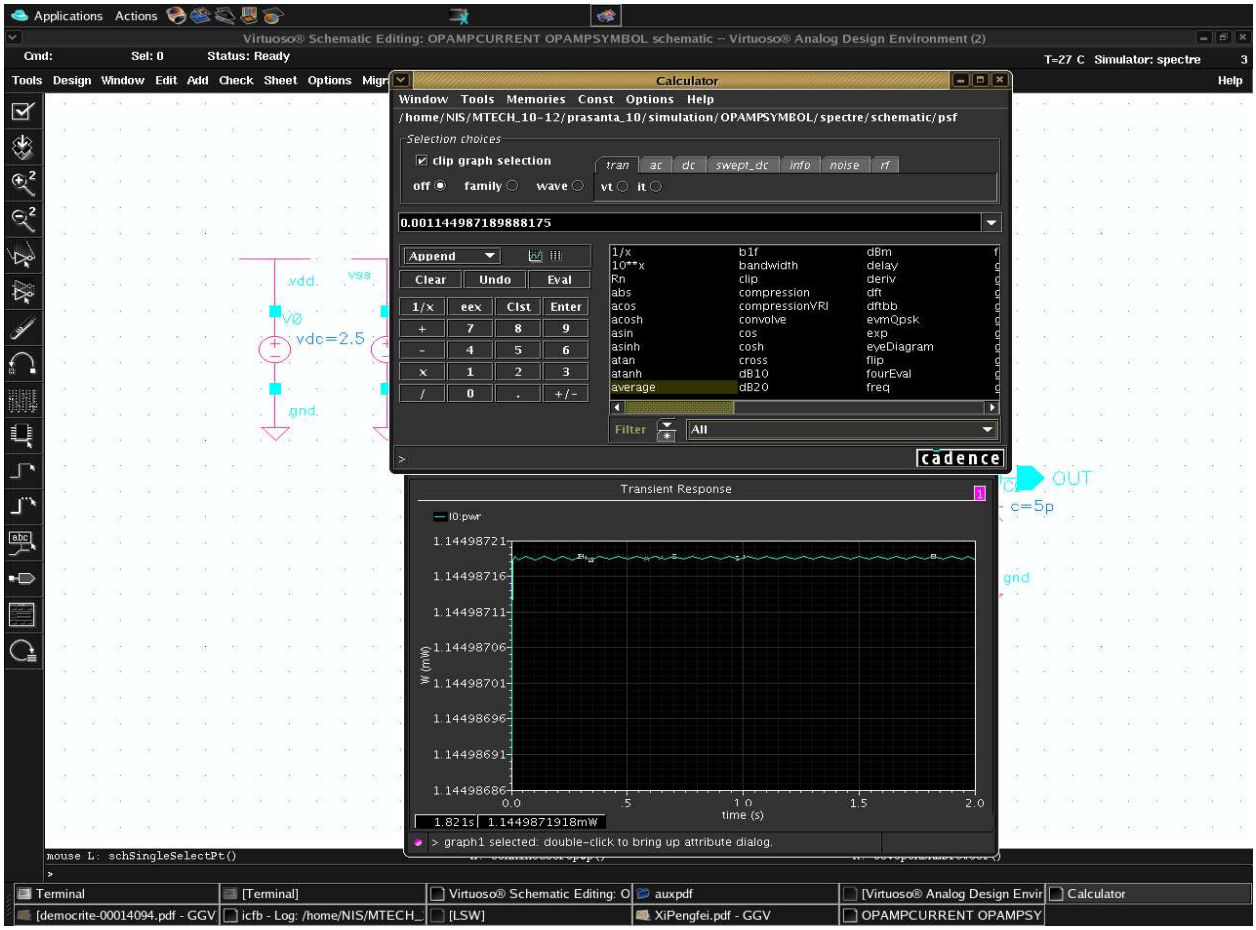

Fig 27: Power consumption of basic opamp.

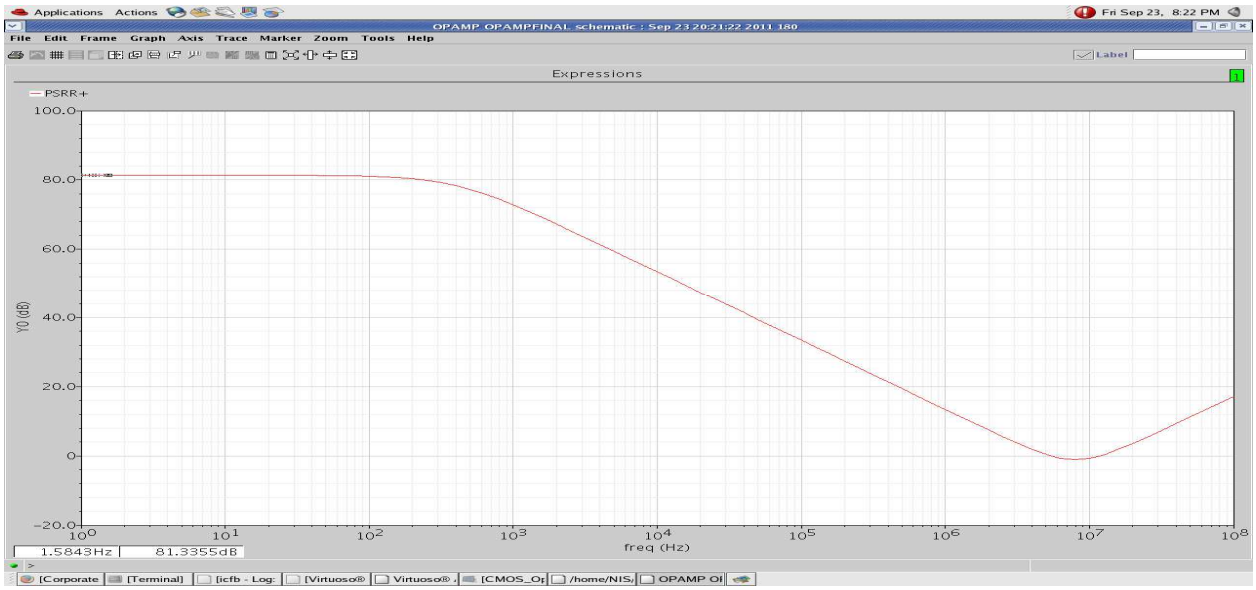

Fig 28: PSRR+ of basic opamp.

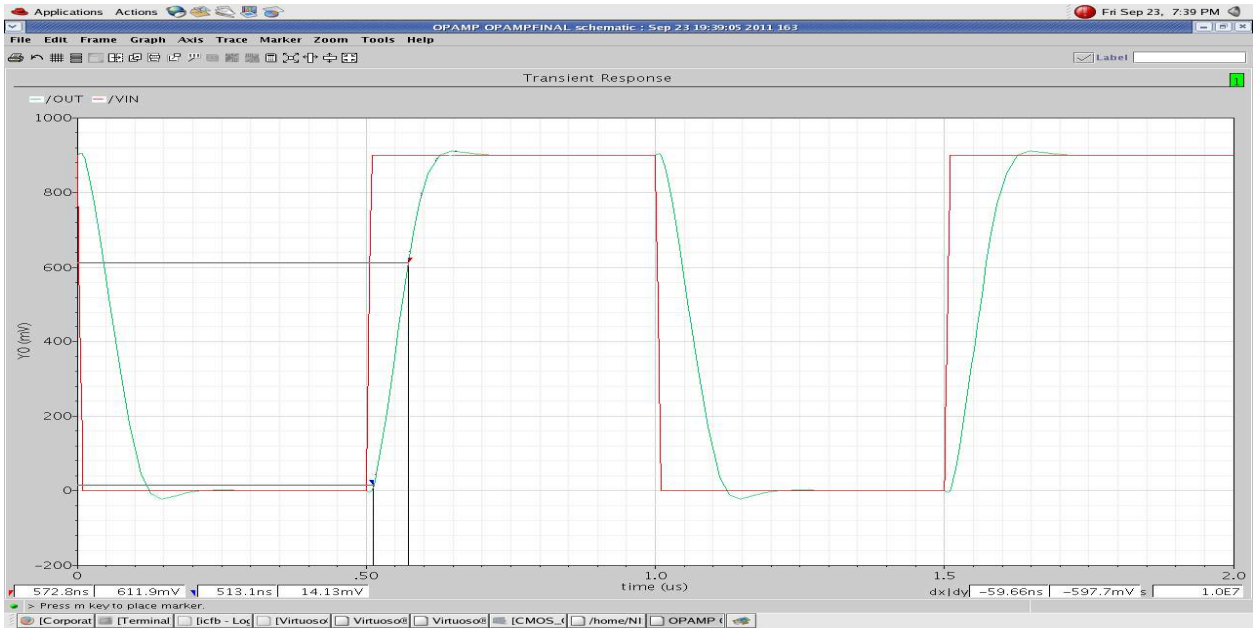

Fig 29: Positive slew rate.

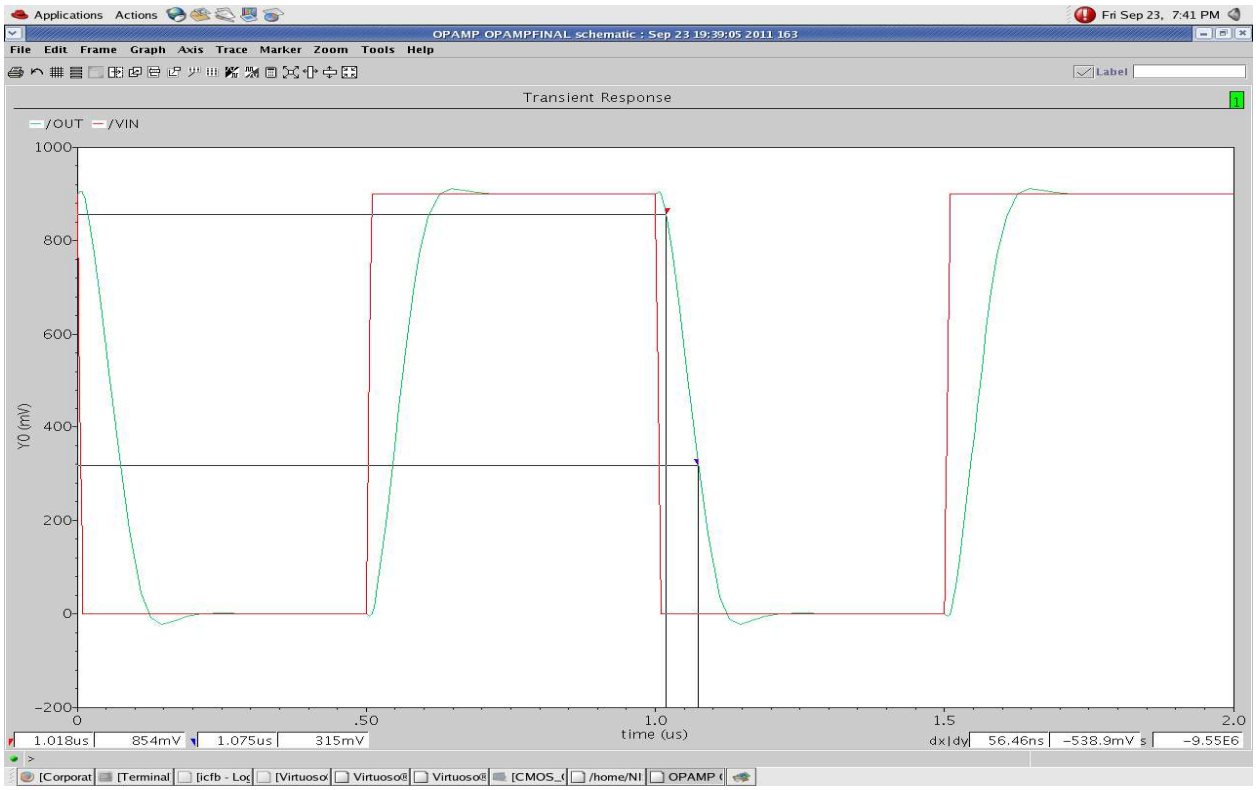

Fig 30: Negative slew rate.

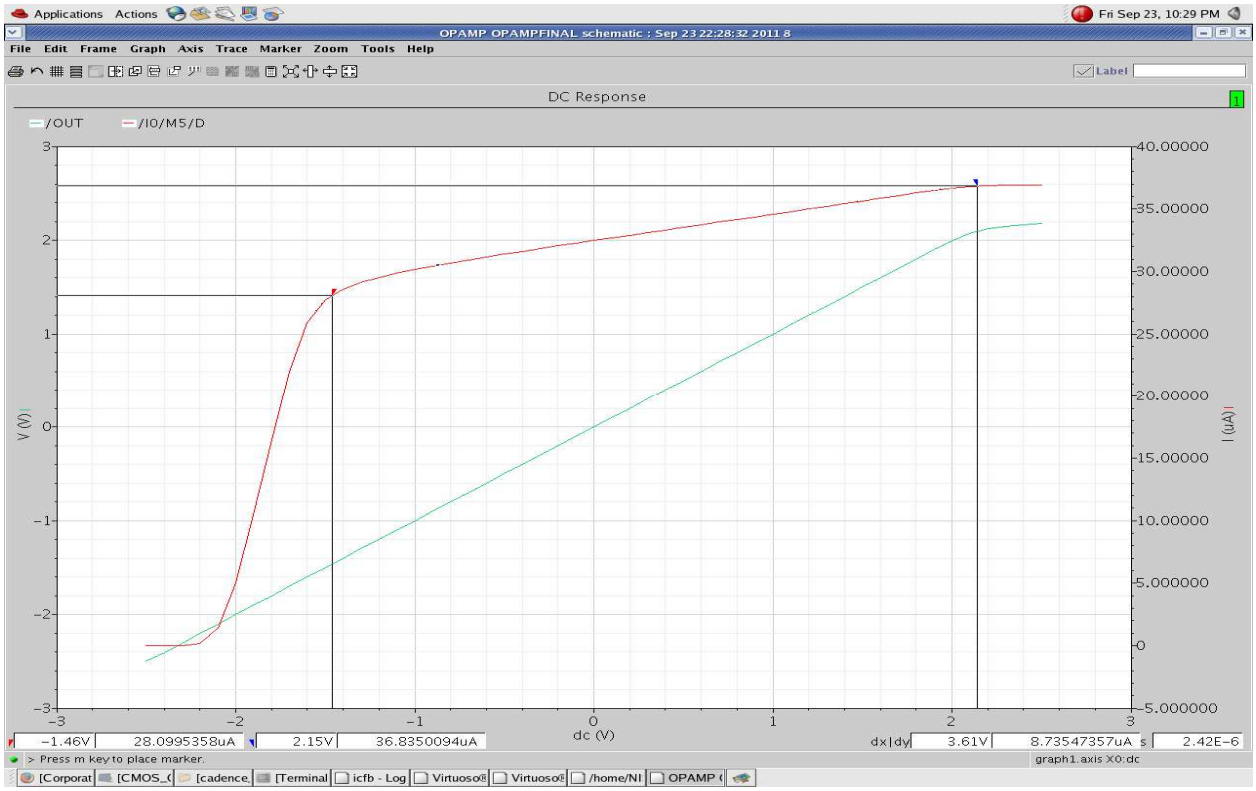

Fig 31: ICMR of basic opamp.

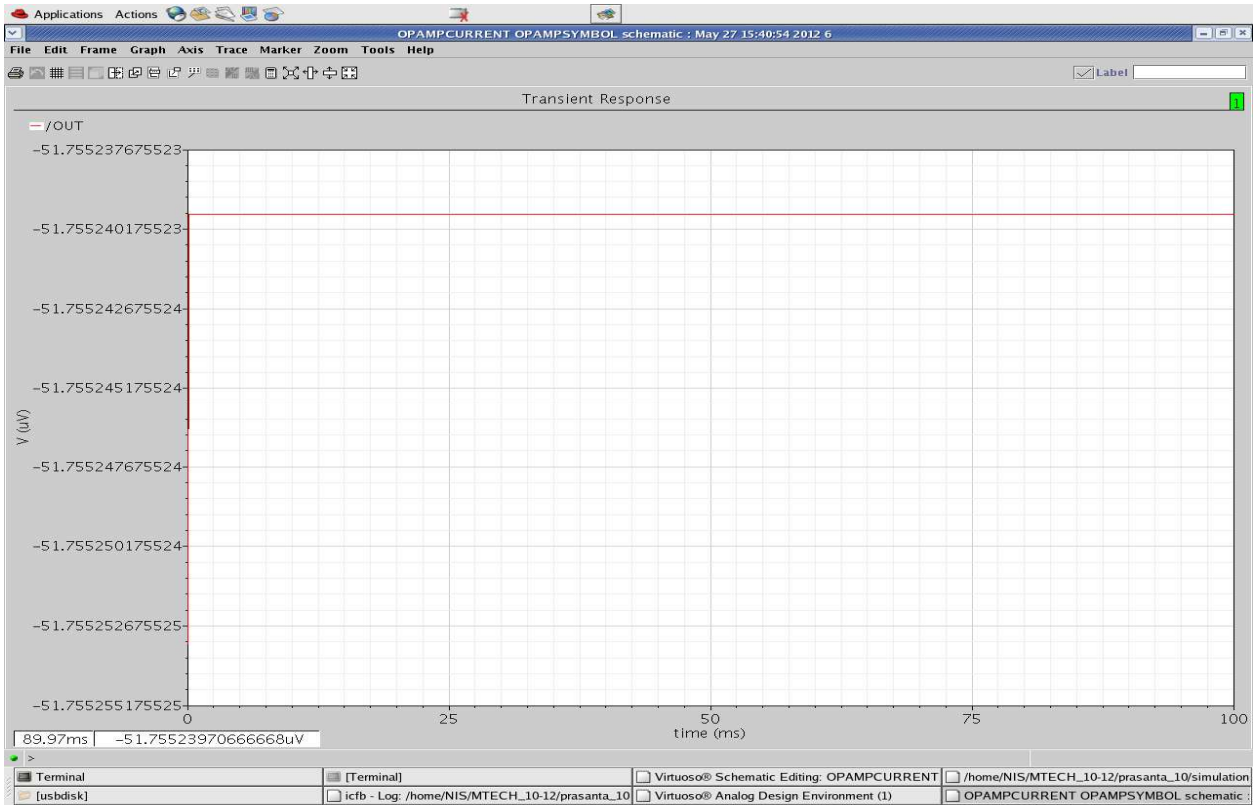

Fig 32: Input offset voltage of basic opamp.

2. Offset of basic and Ping-Pong amplifier comparison

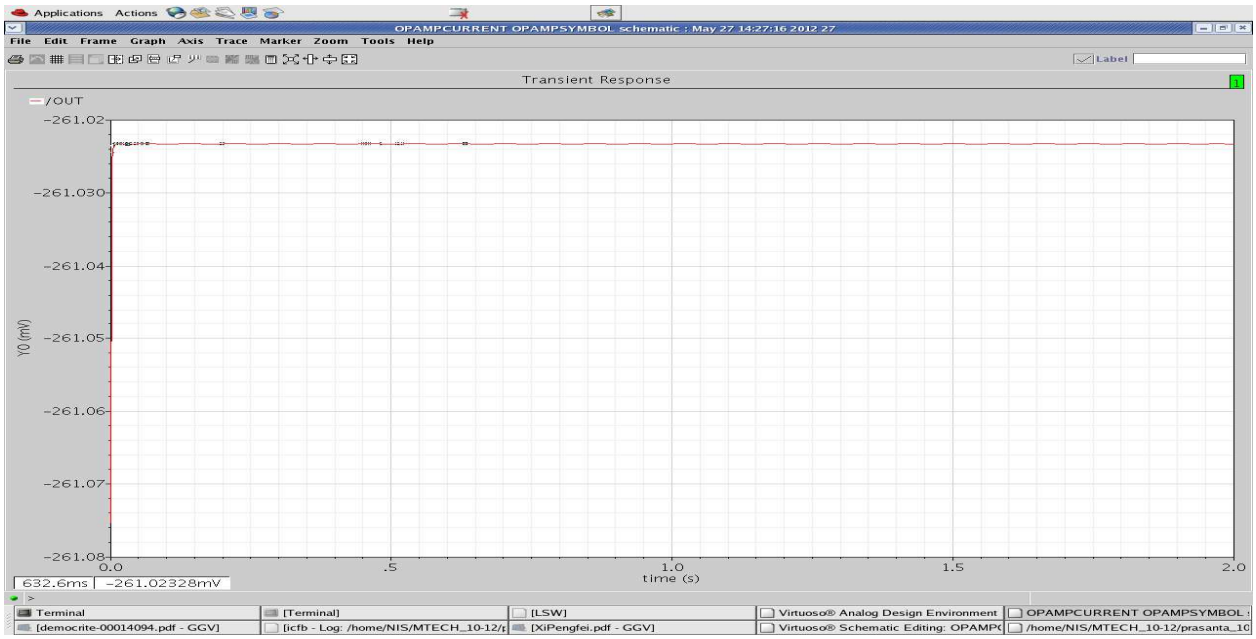

Fig 33: Output offset voltage of basic opamp.

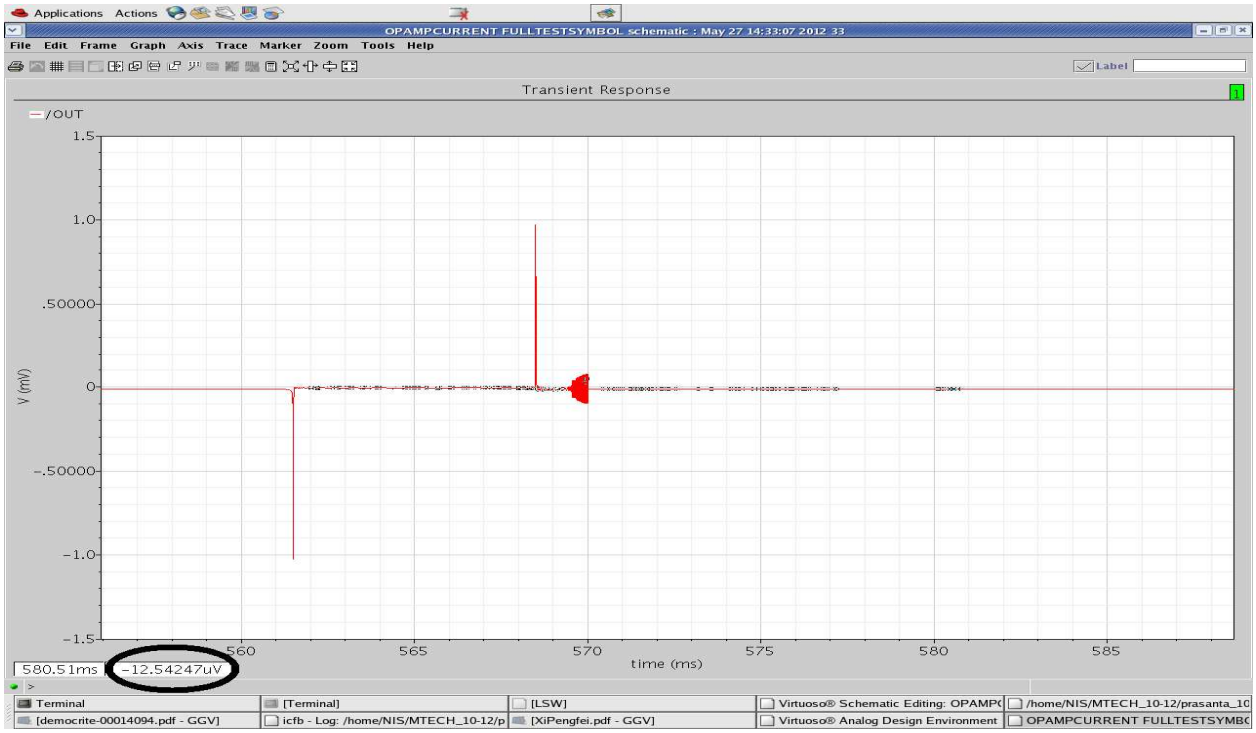

Fig 34: Output offset voltage of Ping-Pong amplifier.

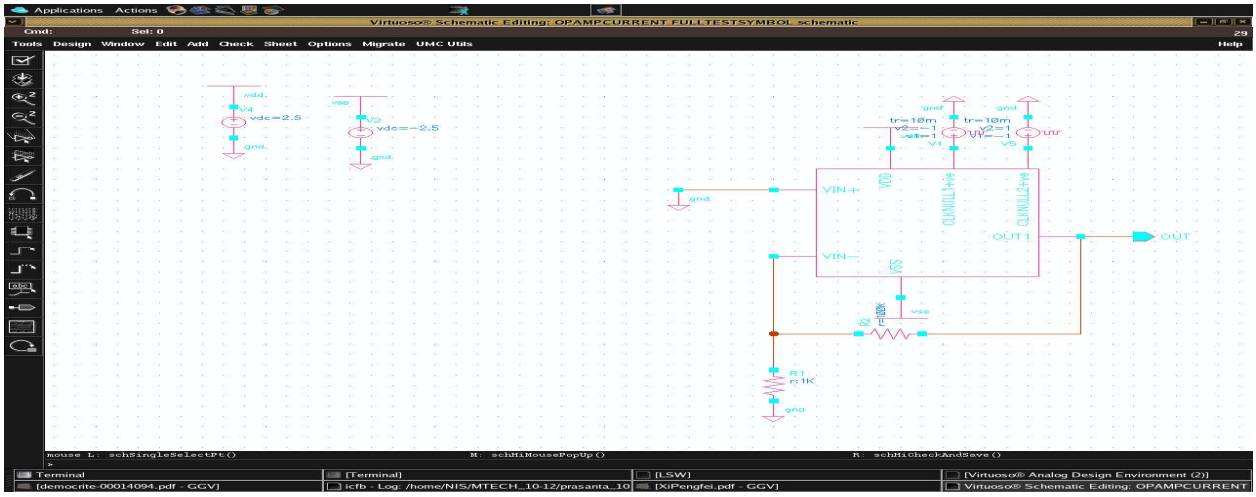

Fig 35: Measurement setup of offset voltage.

3. Offset cancellation of Ping-Pong Amplifier

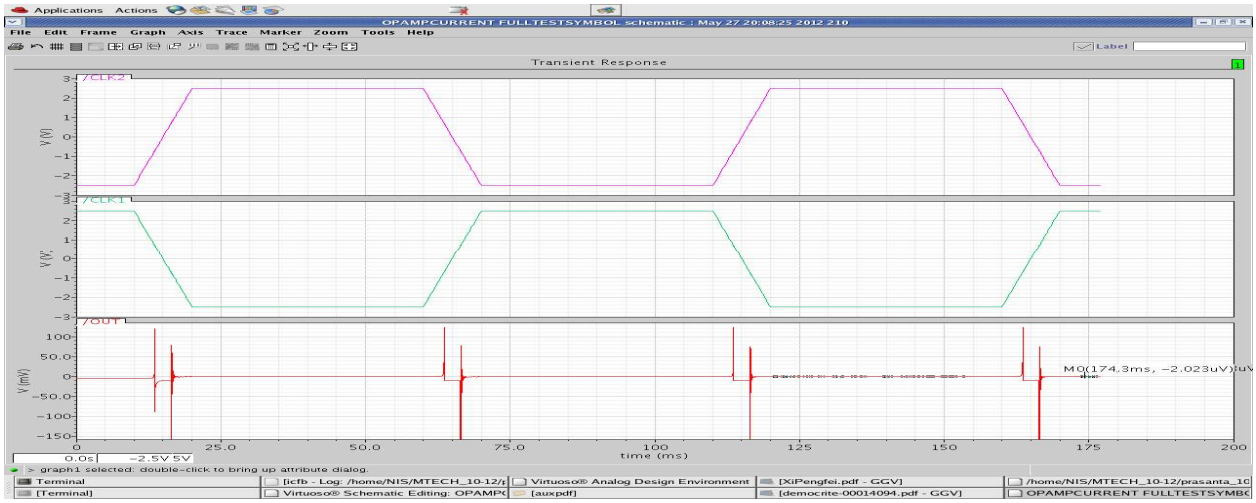

Fig 36(i): Offset cancellation of ping pong amplifier.

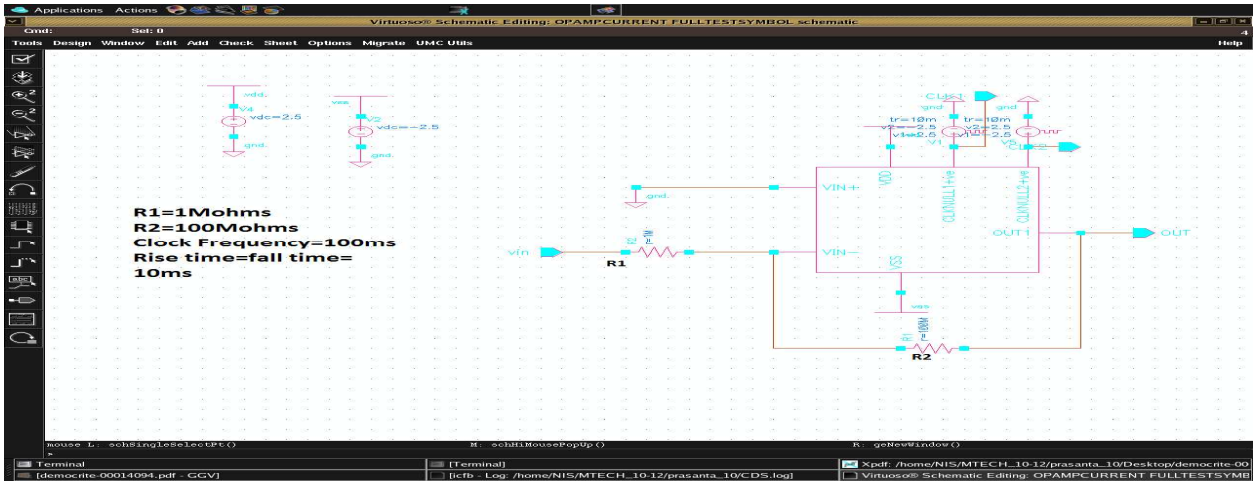

Fig 36(ii): Offset cancellation measurement set up.

An intentional 10 mV of offset is added to one of the inputs (non-inverting) of both the auto zero amplifiers in the ping pong architecture. The simulation result in Fig 36(i) and (iii) shows the offset cancellation is done successfully to an average 4uV during any of the clock phase.

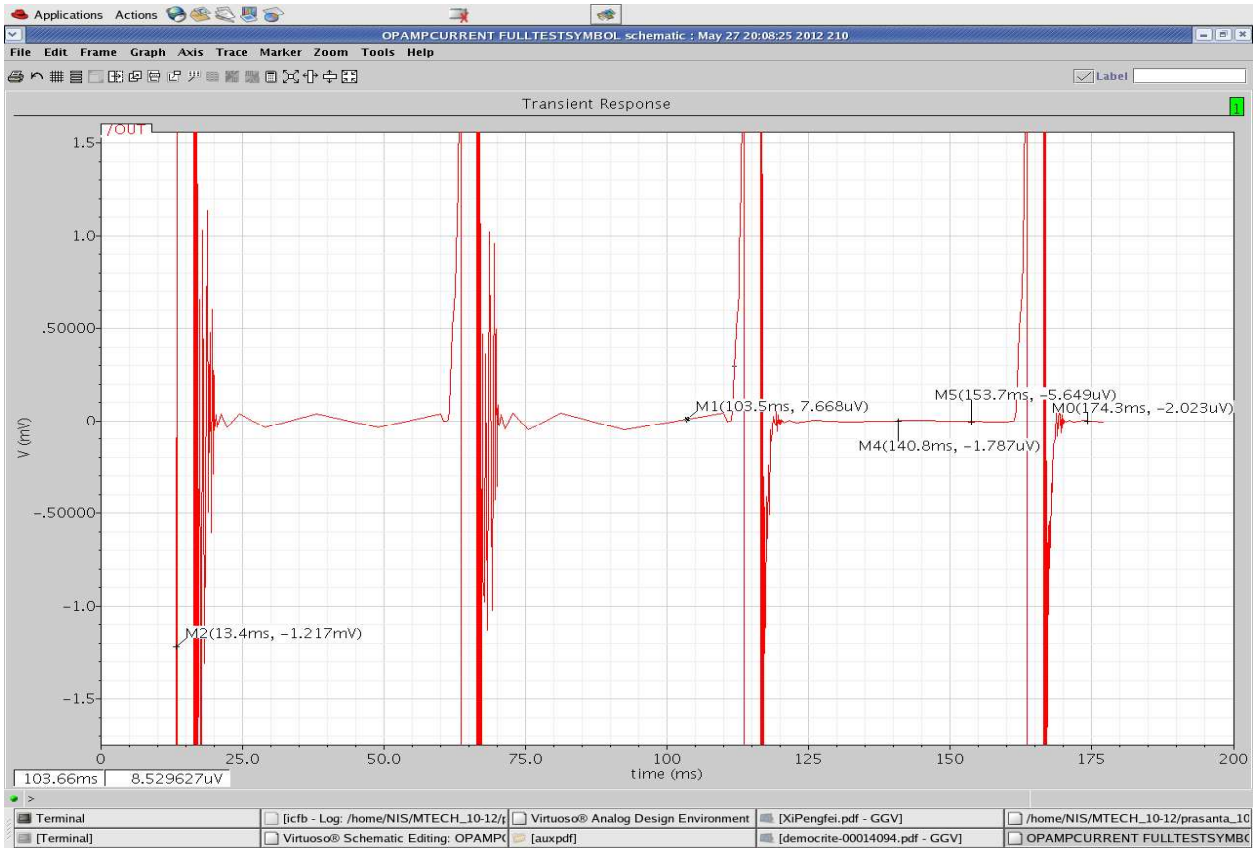

Fig 36(ii): Offset cancellation of ping pong amplifier.

4. Other parameters of Ping-Pong amplifier

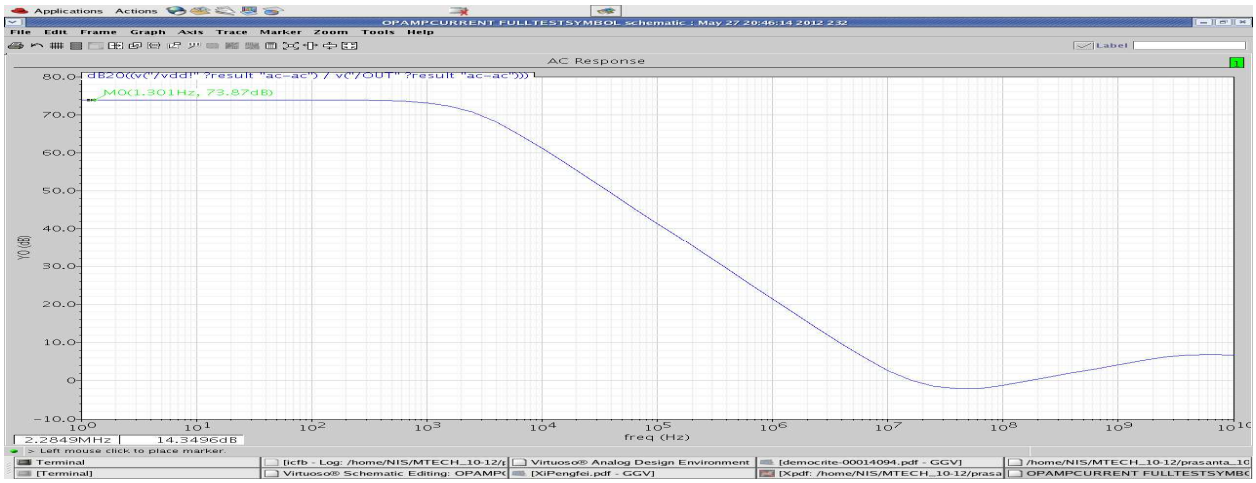

Fig 37: PSRR of ping pong amplifier.

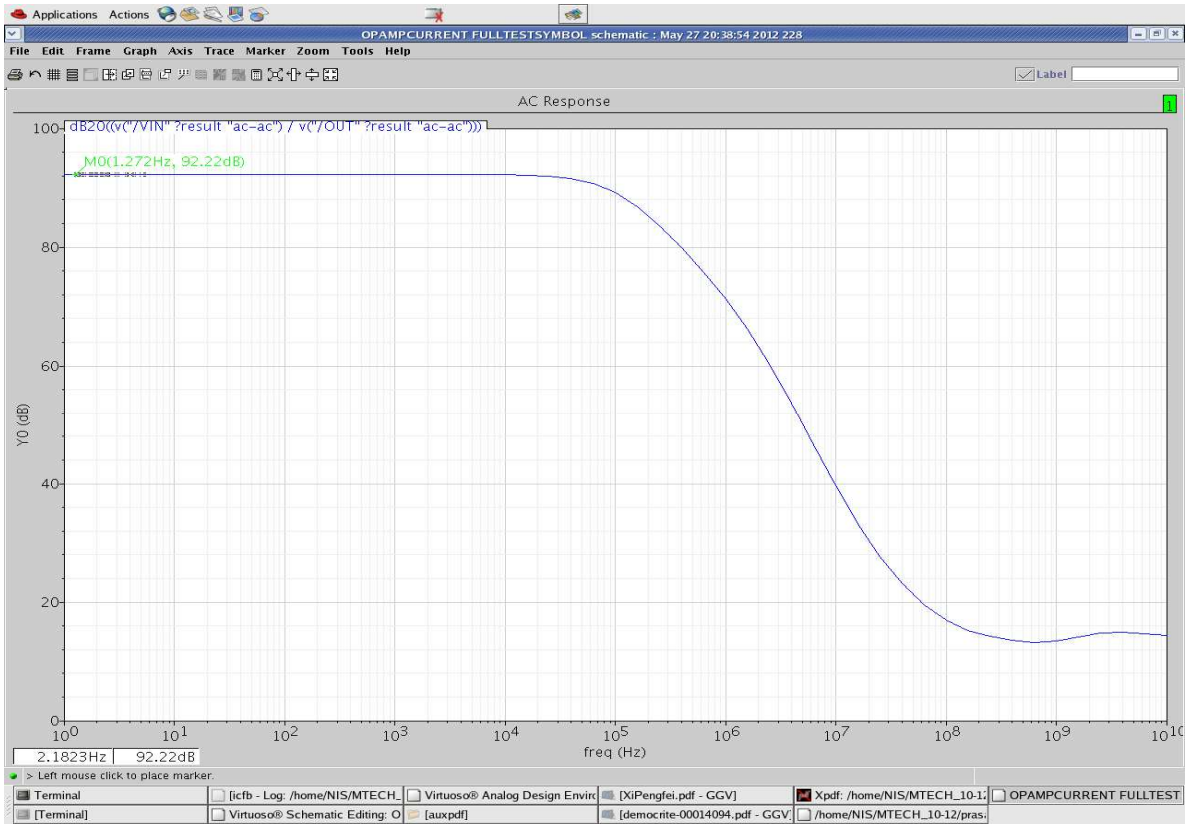

Fig 38: CMRR of ping pong amplifier

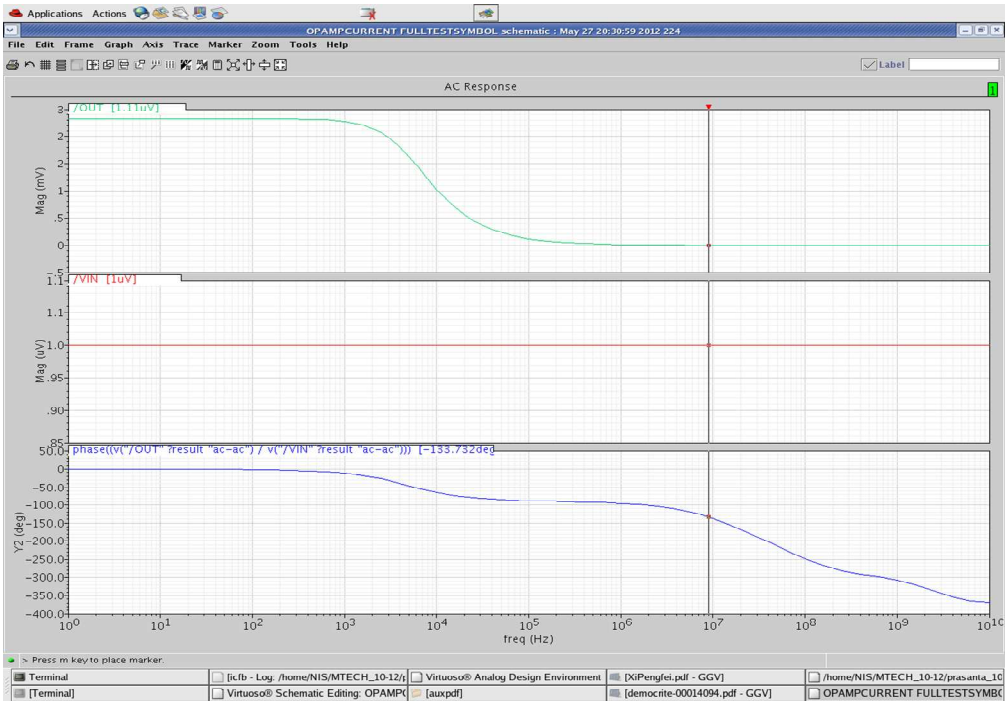

Fig 39: Phase margin of ping pong amplifier.

PM of ping pong amplifier from above diagrams calculated as $47^{0.}$

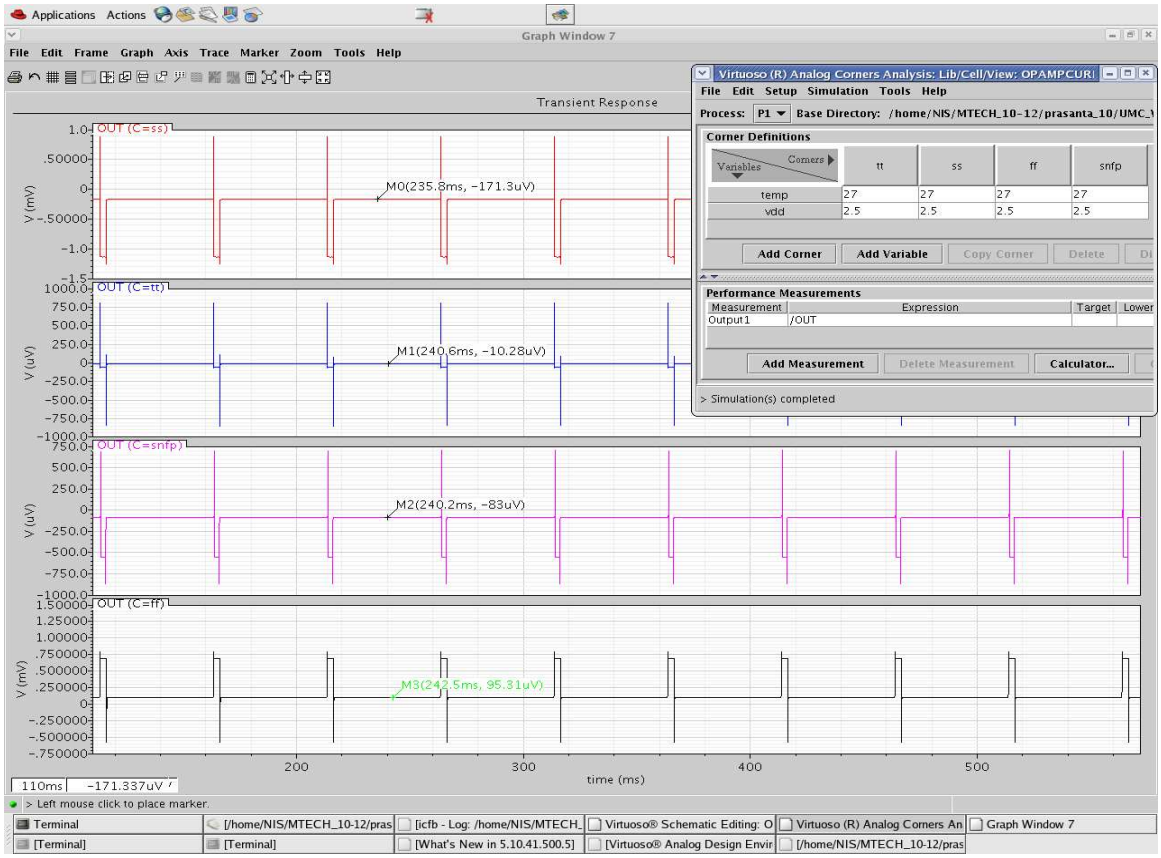

Fig 40: Corner analysis of different models for ping pong amplifier.

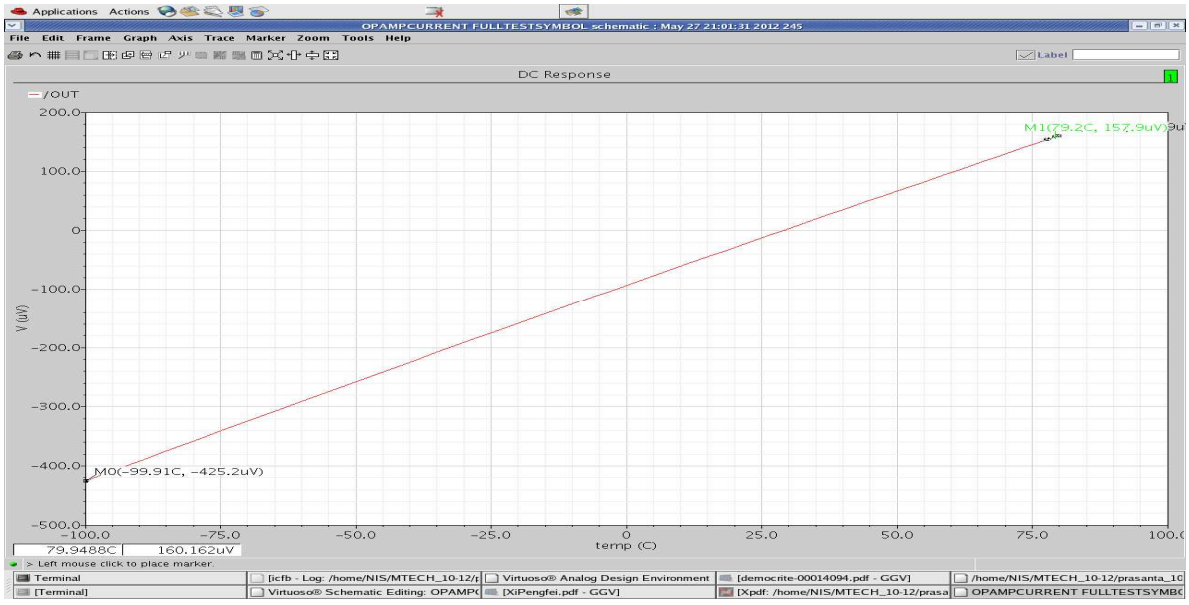

Fig 41: Offset vs. temperature drift of ping pong amplifier.

The temperature drift of offset voltage is found out to be approximately 3.5uV/^{0}C.

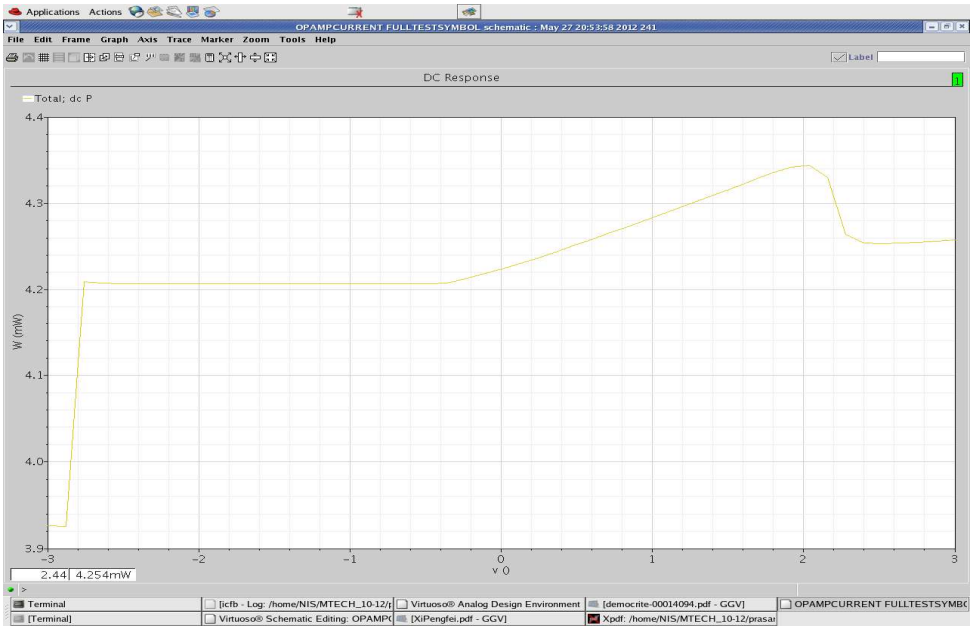

Fig 42: power consumption of ping pong amplifier.

5. Transient Response of Ping-Pong amplifier during Clock Transition period

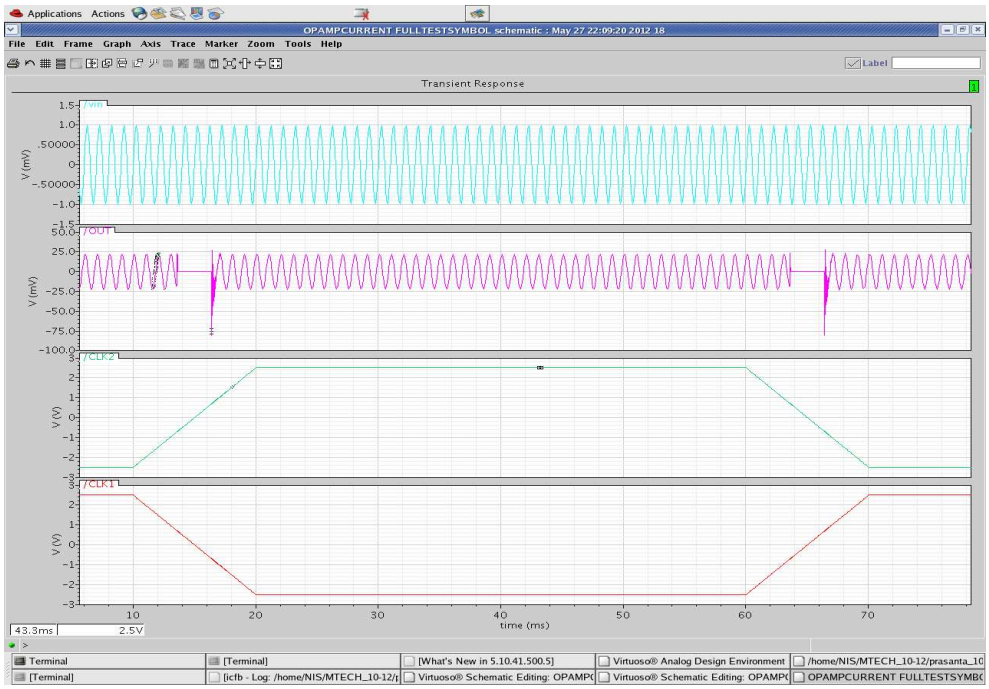

Fig 43**:** Discontinuity of output during clock transition.

The circuit for the above simulation is in non-inverting configuration with R_F = 20M□ and R_{IN} = 1M□.

Conclusion:

The design was tested for very low offset and automatic offset cancellation. It was successfully implemented. But icmr, output ranges were severely affected along with discontinuity of output. Still the gain and the slew rate need to be improved.More accurate switch and S&H circuits with folded cascade opamp architecture will give better results.

References:

[1] Christian C. Enz and Gabor C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceeding of the IEEE*, vol. 84, pp.1584-1614, November 1996.

[2] Ion E. Opris and Gregory T. A. Kovacs, "A Rail-to-Rail Ping-Pong Op-Amp," *IEEE Journal of Solid-State Circuits*, vol. 31, no.9, pp.1320-1324, September 1996.

[3] Stephen C. Terry, Benjamin. J. Blalock, Jeremy R. Jackson, Suheng, Chen, et al, "Development of Robust Analog Electronics at the University of Tennessee for NASA/JPL Extreme Environment Applications," *Proceedings of the 15th Biennial University/Government/Industry Microelectronics Symposium*, pp.124-127, June 2003.

[4] Paul. R Gray, Paul J. Hurst, Stephen H. Lewis and Robert. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, Wiley, 2001

[5] Ron Hogervorst, John P. Tero, Ruud G. H. Eschauzier, and Johan H. Huijsing, "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp.1505-1513, December 1994.

[6] S. Chen, S. C. Terry, C. Ulaganathan, B. J. Blalock, M. M. Mojarradi, "A SiGe Current Reference for Low Temperature Analog/Mixed-Signal Applications," *Seventh International Workshop on Low Temperature Electronics*, June 2006.

[7] D. M. Binkley, B. J. Blalock, and J. M. Rochelle, "Optimizing Drain Current, Inversion Coefficient, and Channel Length in Analog CMOS Design," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 47, no. 2, May 2006, pp. 137-163.

[8] R. L. Greenwell, S. C. Terry, B. J. Blalock, M. M. Mojarradi, and E. Kolawa, "5-V Compatible Radiation-Hardened SOI Rail-to-Rail Input/Output Operational Amplifier for Extreme Environments," *Government Microcircuit Application and Critical Technology Conference*, March 2007.

[9] B. Minch, "A Low-Voltage MOS Cascode Bias Circuit for All Current Levels," *Proceedings of the International Symposium on Circuits and Systems*, vol. III, May 2002

[10] A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," Ph.D. dissertation, University of California, Berkeley, May 1999.

[11] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge Injection in Analog MOS Switches," *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp.1091-1097, December 1987.

[12] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw, 2000

[13] Tony Antonacci and Robert Greenwell, "Opamp Characterization User Reference Manual," July 2006 Edition.

[14] Stephen C. Terry, "Low-Voltage Analog Circuit Design Using the Adaptively Biased Body-Driven Circuit Technique," Ph.D. dissertation, University of Tennessee, Knoxville, August, 2005.

[15] P.E. Allen and D.R. Holberg, CMOS Analog Circuit Design, Oxford University Press: New York, 2002

Appendix A: Layouts

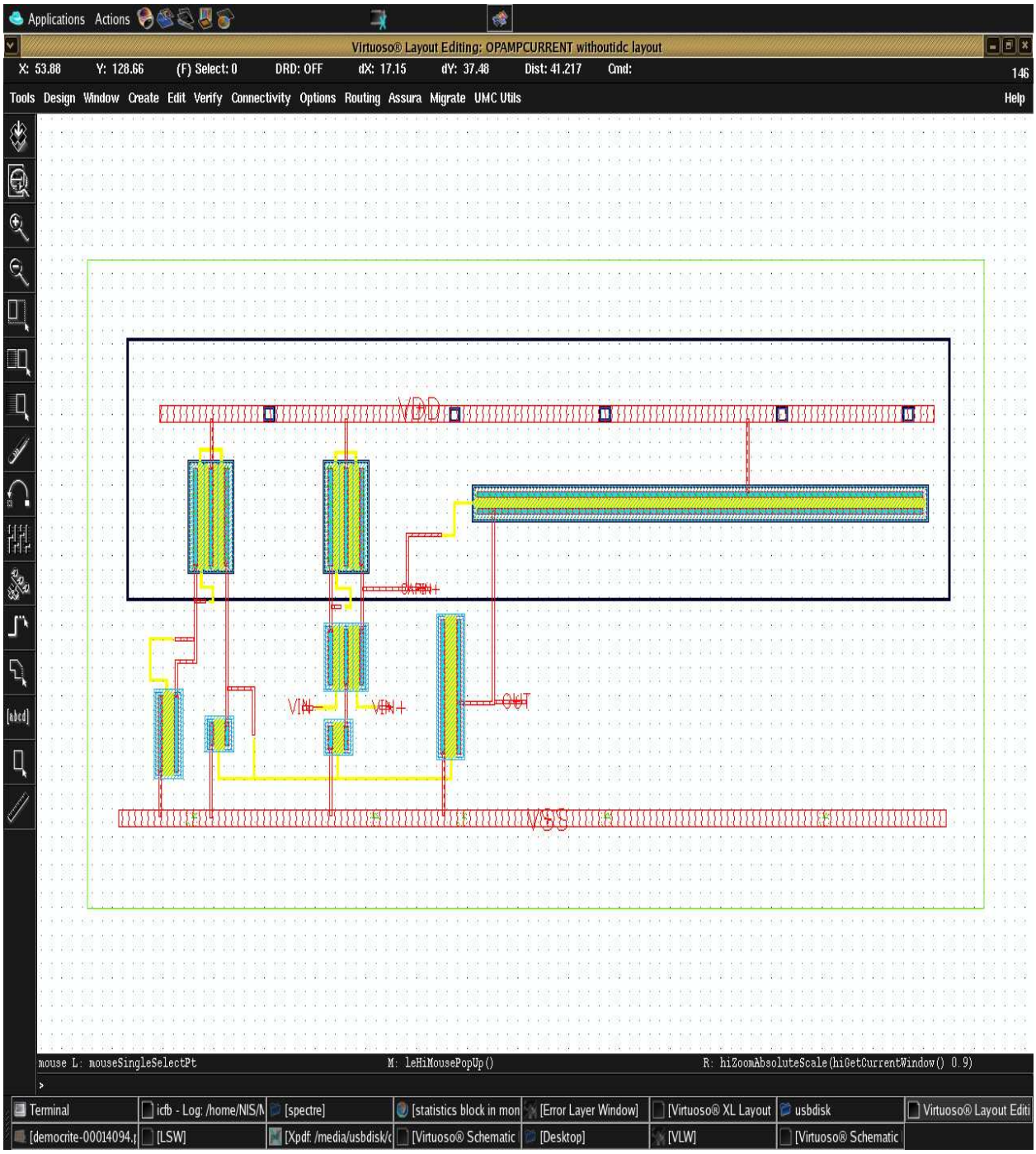

Fig 44: Layout of basic opamp.

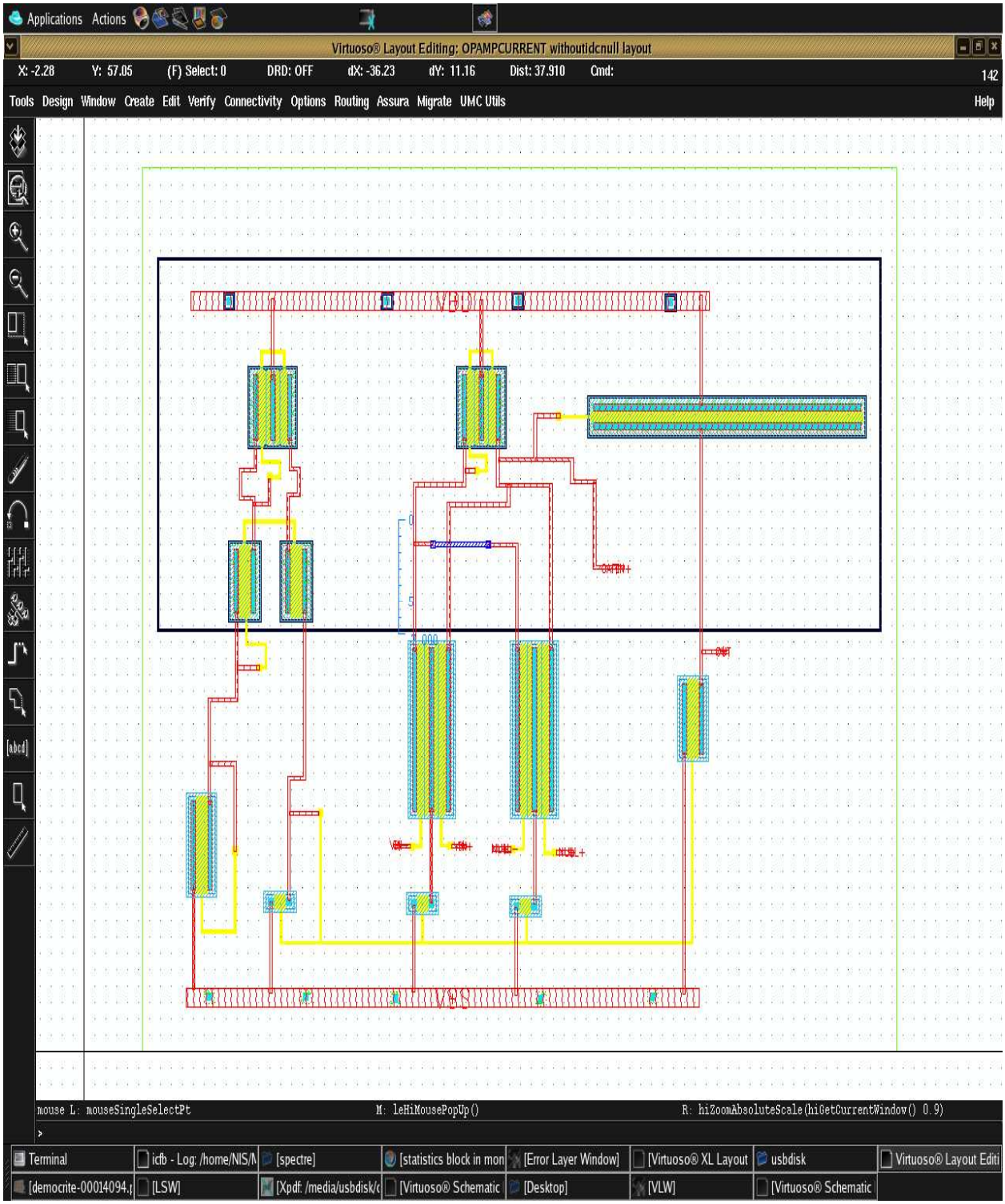

Fig 45: Layout of auto zero opamp (opamp with auxiliary input pair).

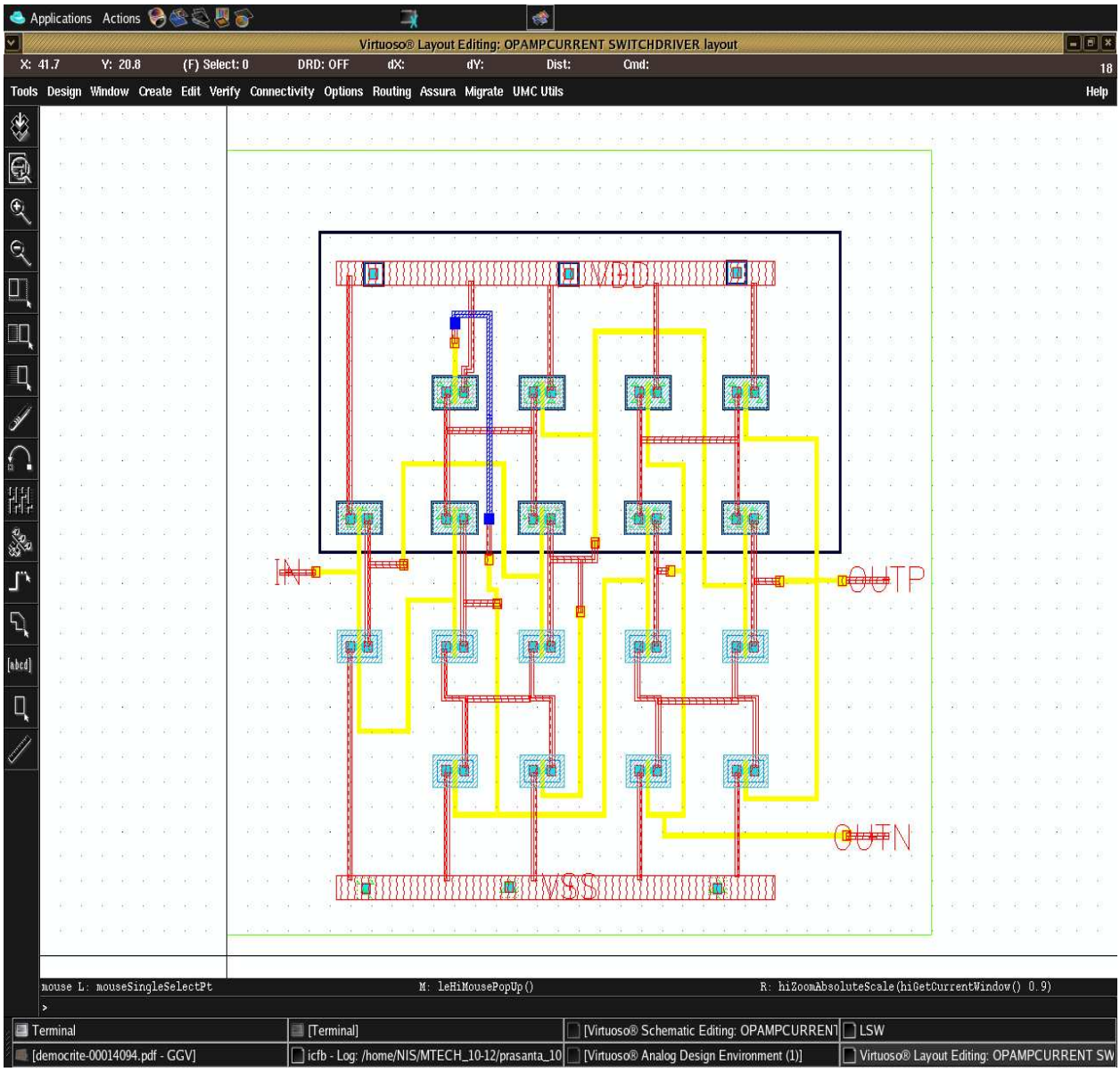

Fig 46: Layout of switch driver.

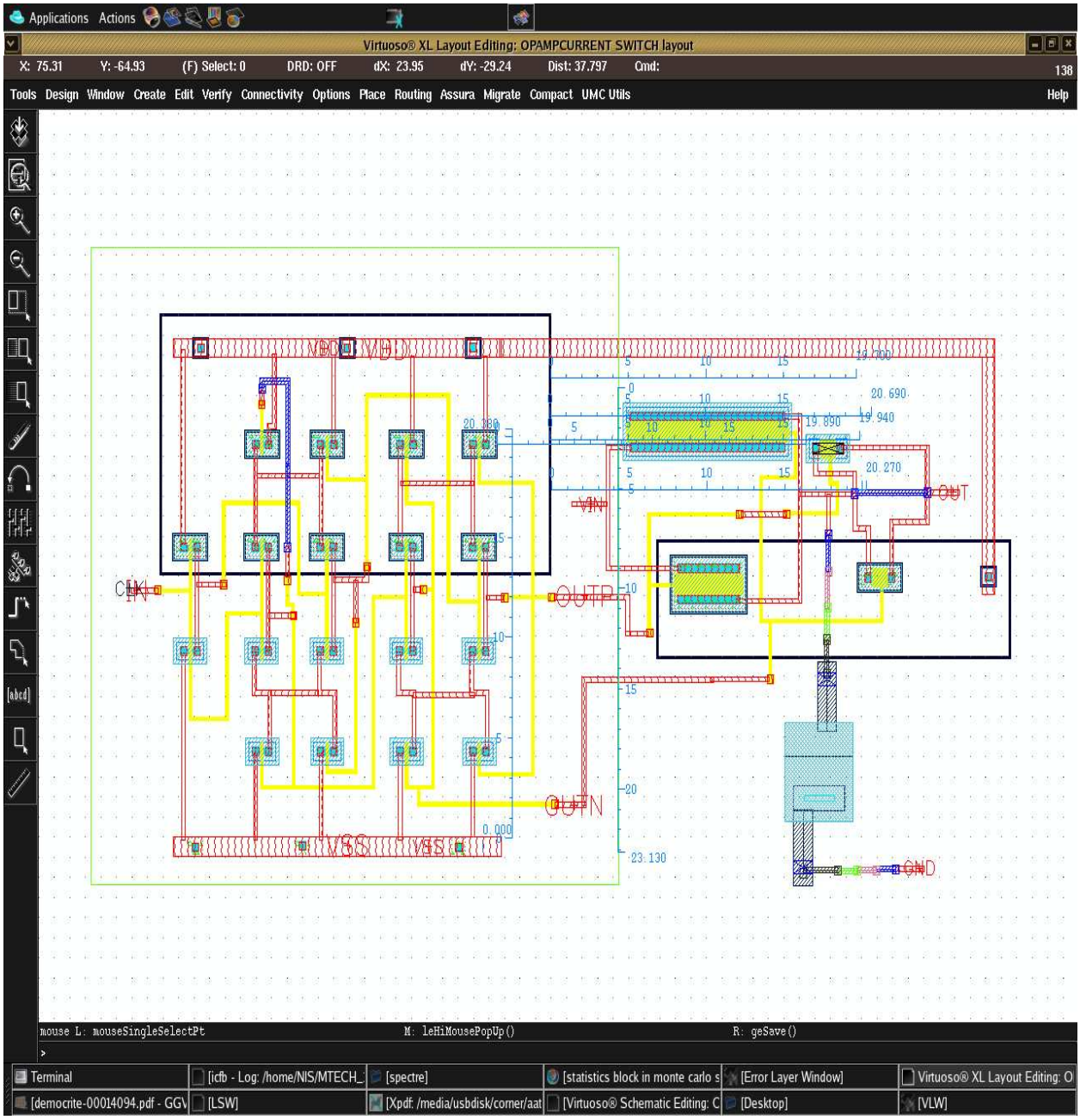

Fig 47: Layout of S&H circuit.

Appendix B: W/L Ratios of Auto zero opamp

$(w/l)_1$, $(w/l)_{aux1}$	10
$(w/l)_2$, $(w/l)_{aux2}$	10
$(w/l)_5$, $(w/l)_{aux5}$	0.4
$(w/l)_3$	4
$(w/l)_4$	4
$(w/l)_6$	40.83
$(w/l)_7$	4.36
$(w/l)_8$	0.4

Fig 48: W/L Ratios of opamp using auxiliary input port.

The above sizes are determined as per the specifications mentioned in Table 4.